CS 203 (2020 Fall) Assignment #3

Student ID #:

Name:

Who else you discussed with when finishing the assignment:

(While you may have your partner do all the work, this will only hurt you when the midterm and final come around so don't do it.)

* For your answer to each question, please clearly specify what formula you use to solve the problem before replacing each term with numbers.

* Please show your work as detailed as possible.

* We refuse to give credits for answers with only final results even they are correct.

1. Consider the following RISC-V instructions:

```
Loop:   LD     X1,0(X3)
        ADD    X2,X1,X4
        MUL    X1,X2,X6
        ADD    X1,X1,X5
        ADD    X7,X7,X1
        ADDI   X12,X12,-1
        BNEZ   X12,Loop
        ADDI   X16,X16,4
        LD     X3,0(X16)
```

   Assume the initial value of X12 is 2. Please answer the following question.

   (1) Assume the branch instruction is in the BTB and the branch is always predicted taken. Please list the instruction sequence that will be **executed** (an instruction that does not finish until the end does not count).

(2) Continued from the previous question, if you have a 5-stage RISC-V pipeline as in Figure C.25 of the textbook, can you draw the pipeline diagram that simulates the execution of the above instructions sequence? You may use the given table for the diagram.

WB															
ME															
EX															
ID															
IF															
LD X1,0(X3)															

2. You are building a system around a single-issue in-order processor running at **2 GHz** and the processor has a base CPI of 1 if all memory accesses are hits. The only instructions that read or write data from memory are loads (20% of all instructions) and stores (5% of all instructions). The processor uses virtually-indexed, physically-tagged caches with no penalty in address translation if the TLB access is a hit. However, if the TLB misses, the system needs 120ns to finish the address translation and TLB updates. The TLB miss rate is 2%. The L1 cache is split into I-cache and D-cache with no penalty on hits. Both the I-cache and D-cache are direct mapped and hold 32KB each. You may assume the caches use write-allocate and write-back policies. The L1 I-cache has a 2% miss rate and the L1 D-cache has a 5% miss rate. Also, 50% of all blocks replaced from L1 D-cache are dirty. The 512KB write-back, unified L2 cache has an access time of 10ns. Of all memory references sent to the L2 cache in this system, 80% are satisfied without going to main memory. Also 25% of all blocks replaced are dirty. The main memory has an access latency of 60ns. What is the overall CPI, including memory accesses?