CS 203 (2020 Fall) Assignment #4

Student ID #:

Name:

Who else you discussed with when finishing the assignment:

(While you may have your partner do all the work, this will only hurt you when the midterm and final come around so don't do it.)

* For your answer to each question, please clearly specify what formula you use to solve the problem before replacing each term with numbers.

* Please show your work as detailed as possible.

* We refuse to give credits for answers with only final results even they are correct.

1. You are asked to evaluate the performance of the following branch prediction schemes:

   A: Static backward taken, forward not taken.

   B: Local predictor with two-bit state machine (Saturating counter/Bimodal).

   C: Global predictor based on 4-bit history and a 2-bit state machine associate with each entry. (4,2) correlating predictor.

   Now, you are given the following code segment. Assume each of the branch PC never cause conflicts/alias with other branches and the predictors are initialized as all zeros. Please evaluate the branch prediction accuracy for the following code snippet with all the give prediction schemes.

   (1)
```
int i, j;

i = 0;
do {
    j = 0;
    do {
        loop c[i][j] = a[i][j] + b[i][j];
    } while( ++j < 5);
} while ( ++i < 100);
```

(2)
```
int i, j;

    i = 0;
    do {
        j = 0;
        do {
            loop c[i][j] = a[i][j] + b[i][j];
        } while( ++j < 2);
    } while ( ++i < 100);
```

2. Consider the following RISC-V instructions:

```
Loop:   LD     F1,0(X3)
        ADD.D  F2,F1,F4
        MUL.D  F1,F2,F6
        ADD.D  F1,F1,F5
        ADD.D  F7,F7,F1
        ADDI   X12,X12,-1
        BNEZ   X12,Loop
        ADDI   X16,X16,4
        LD     X3,0(X16)
```

Assume the initial value of X12 is 2. Please answer the following question.

(1) Assuming that you are given a processor using Tomasulo algorithm for instruction scheduling. The execution time and reservation stations for each functional unit is listed as below:

Functional units	Execution time	Reservation Stations
INT ALU	1	
FP ADD	2	
FP MUL	3	
Memory Access	1	4 for Address Calculation, 3 for loads, 3 for stores
Branch	1	

Please draw the pipeline diagram according to the Tomasulo handout
http://cseweb.ucsd.edu/classes/wi10/cse240a/Slides/tomasulo.pdf
for the given code.

(2) Assuming that you are using an Alpha 21264-Like processor (i.e. register renaming) that is very similar to a real Alpha 21264 except the processor has the same function unit execution time and branch predictor as the previous problem. Please draw the pipeline diagram for the given code. (You may assume the processor has the same number of functional units as the previous problem. Ignore the functional unit cluster problem and assume there are bypass paths for memory and ALU operations).

(3) Assuming R2 is very large, which of the above performs better and why?