First Day of CS203: Advanced Computer Architecture

Hung-Wei Tseng

Before we get there …

CS203 Fall 202

Welcome to the first CS203 after
wear our masks during the whole
few questions that I need to colle
lecture.

This form is automatically collec

What's your name?

I am a …

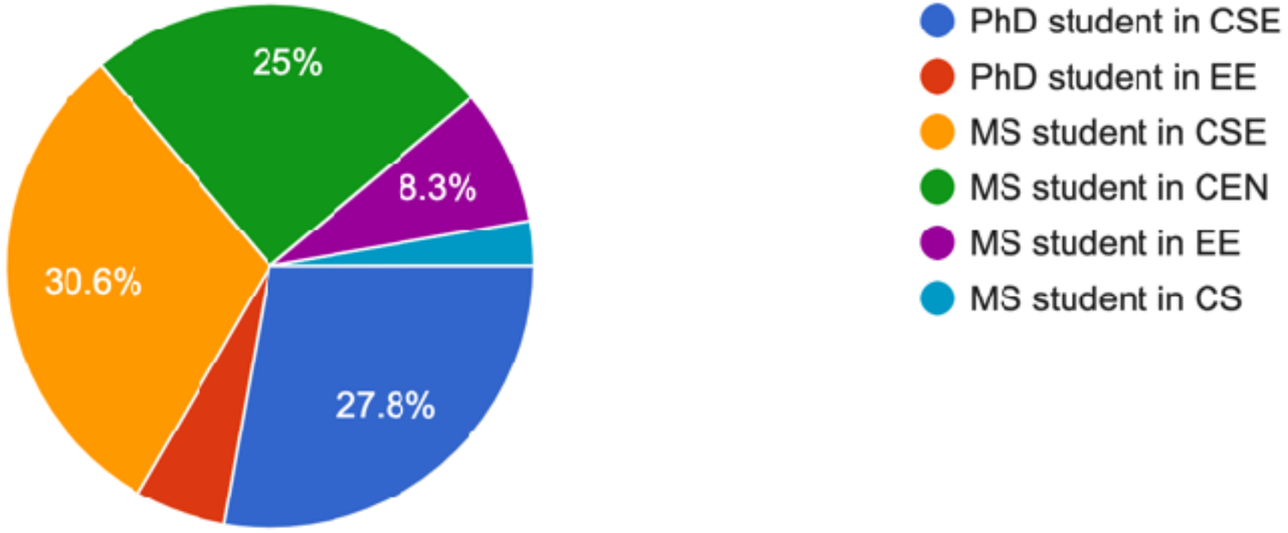
PhD student in CSE

ssa.gov/cact/babynames/decades/centu…

10 most popular boy names in Arab

I am a …

36 responses



前年度：6位

3 蓮 れん 件数：108 占有率：0.56%

前年度：8位

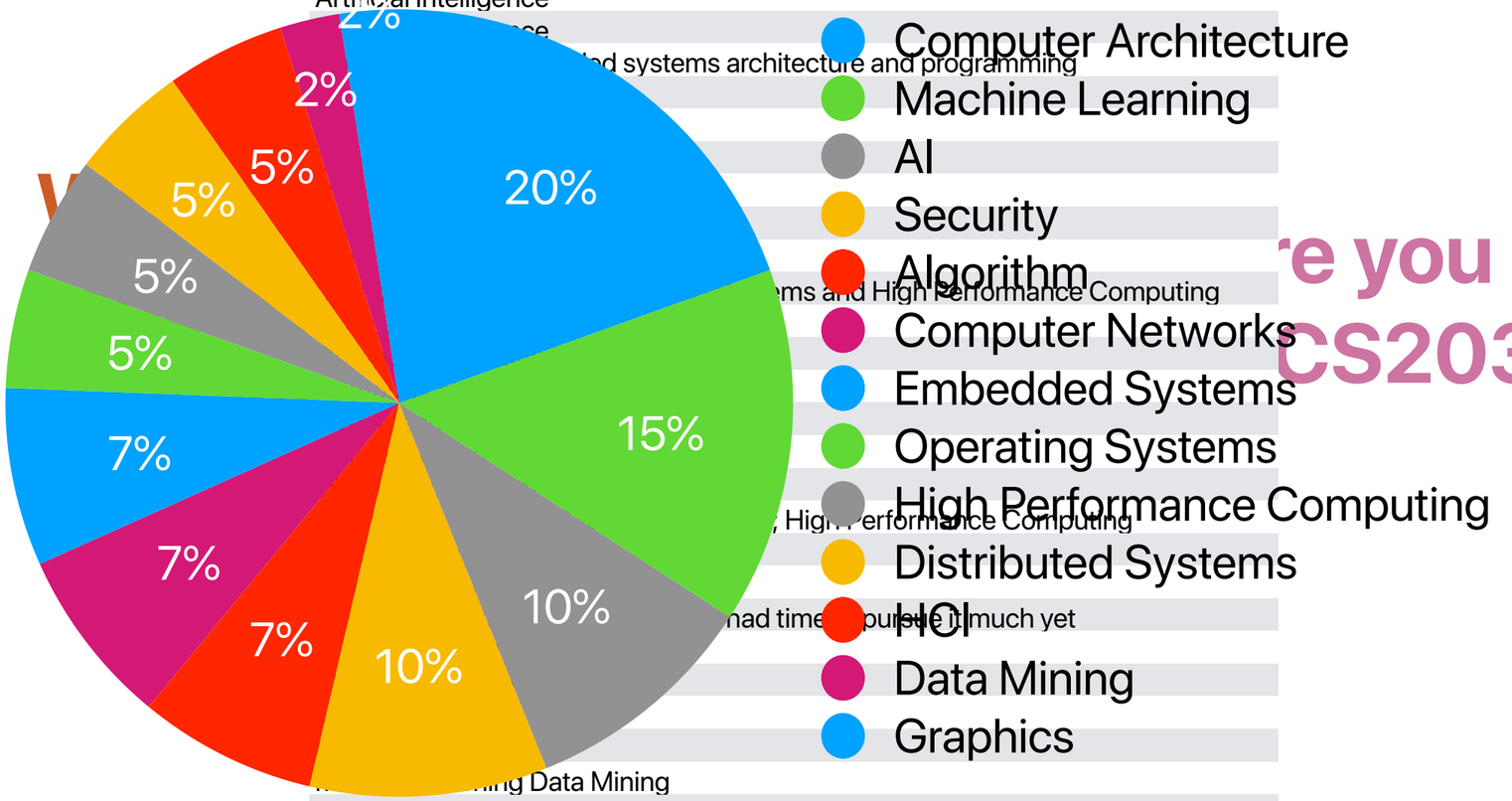
3 陽菜 ひな 件数：115 占有率：0.64%

麗華
淑娟
淑卓

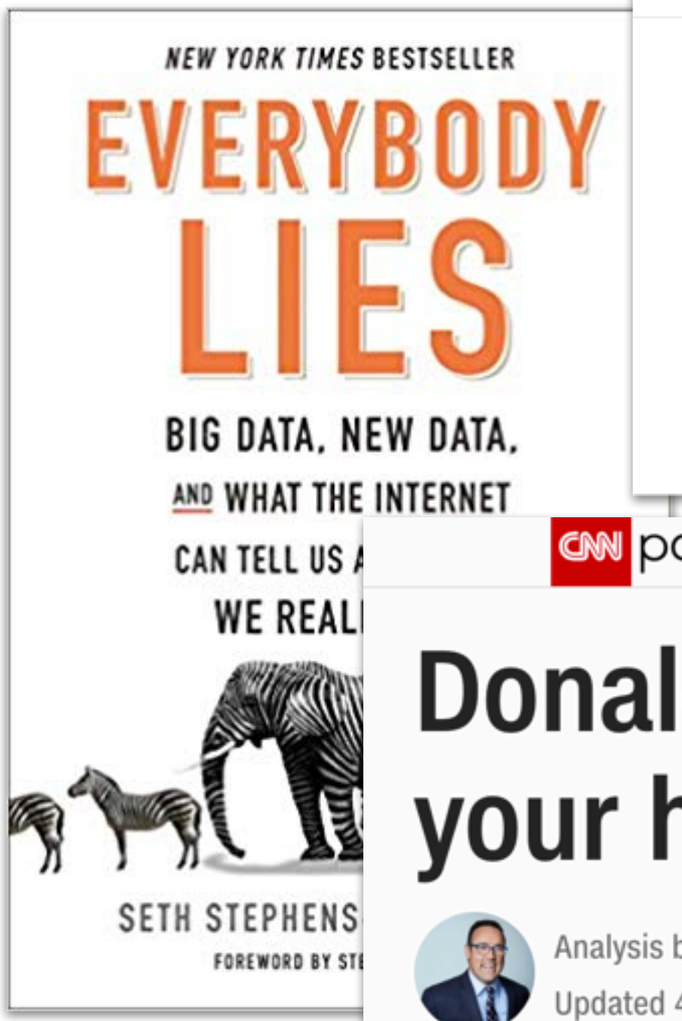
Before we get there ...

What's your name?

AI & human computer interactions
algorithm
algorithm
algorithm design
Artificial Intelligence
[illegible] systems architecture and programming
[illegible] ms and High Performance Computing
[illegible] High Performance Computing
[illegible] nad time [illegible] pursue it much yet
[illegible] ning Data Mining
Machine Learning, AI
Networking
OS
Security and Privacy (S&P)
Security, Fuzzing
Software Dev, Comp Security
Towards the computer hardware



[illegible] e you CS203



Google

How Often Do People Lie

All News Images Videos Shopping More Settings Tools

About 267,000,000 results (0.54 seconds)

The study, published in the journal's June issue, found that 60 percent of **people lied** at least once during a 10-minute conversation and told an average of two to three lies. "**People** tell a considerable number of lies in everyday conversation. Jun 10, 2002

UMass researcher finds most people lie in everyday ...
https://www.eurekalert.org › pub_releases › uoma-urf061002

CNN politics 45 Congress SCOTUS Facts First 2020 2019 Elections LIVE TV Edition

Donald Trump lies more often than you wash your hands every day

Analysis by Chris Cillizza, CNN Editor-at-large
Updated 4:56 PM ET, Mon June 10, 2019

Before we get there …

What's your name?

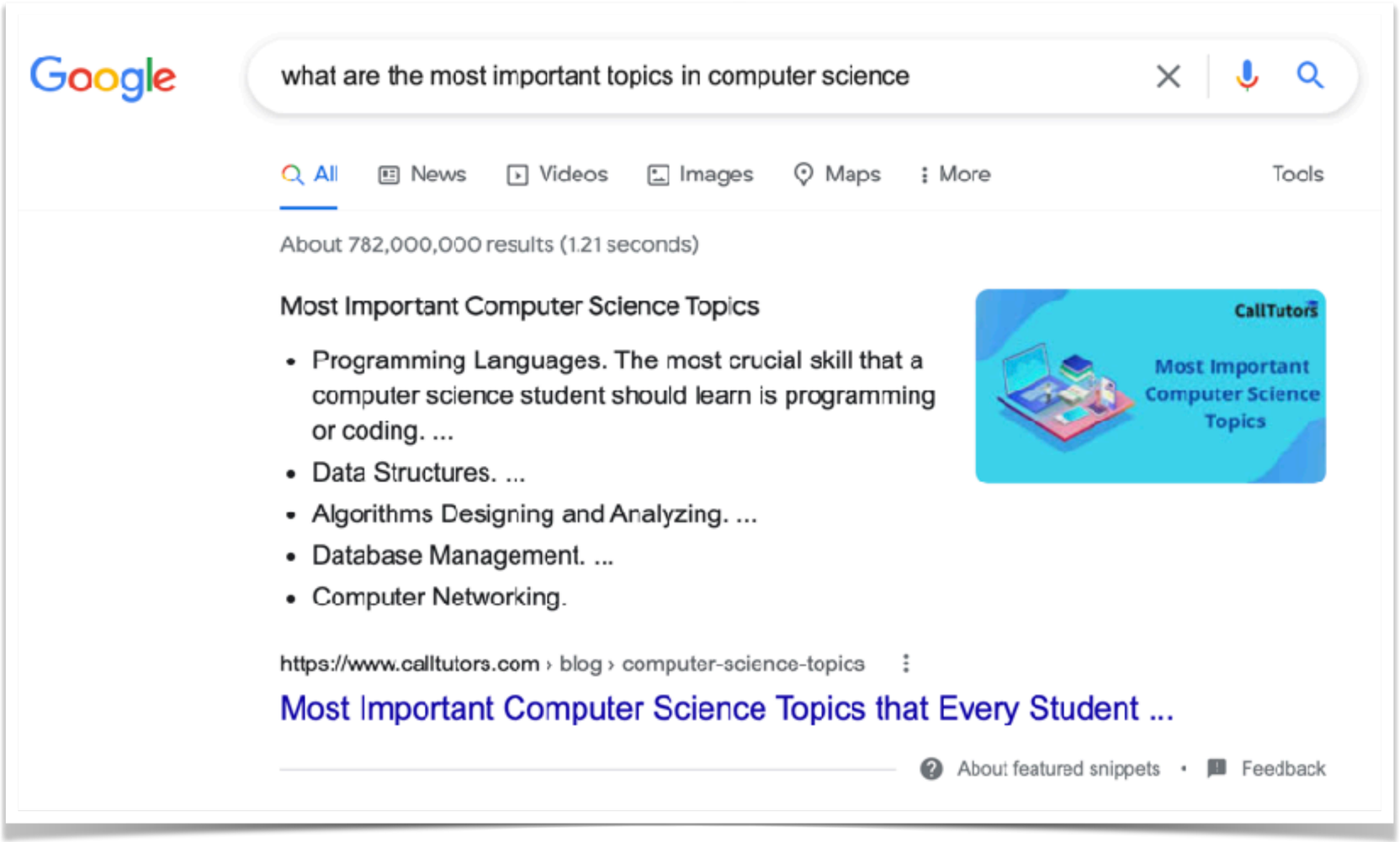
You want to understand the underlying workings and design of modern computers

I am interested in this topic

I want to learn more about computer architecture

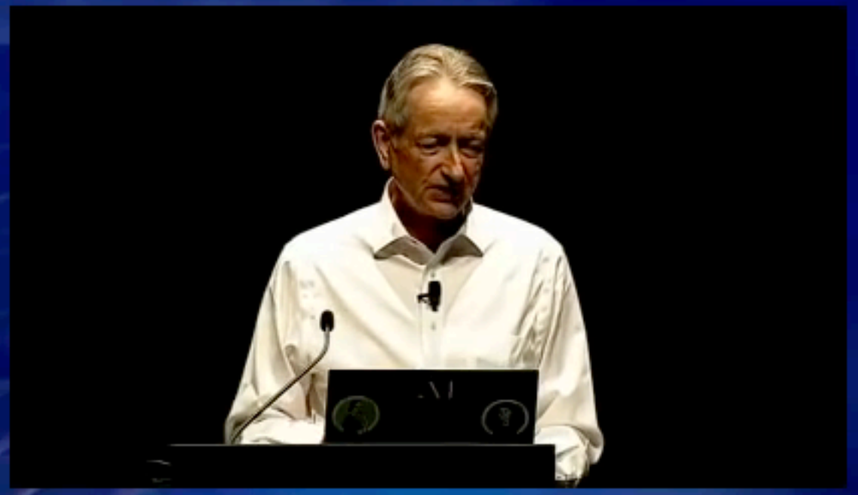
Before we get there …

What's your favorite topic in computer science?



The return of backpropagation

- Between 2005 and 2009 researchers (in Canada!) made several technical advances that enabled backpropagation to work better in feed-forward nets.
  - Unsupervised pre-training; random dropout of units; rectified linear units.
  - The technical details of these advances are very important to the researchers but they are not the main message.
  - The main message is that backpropagation now works amazingly well if you have two things:
    - a lot of labeled data
    - a lot of convenient compute power (*e.g.* GPUs)



acm FCRC

2018 ACM A.M. Turing Lecture

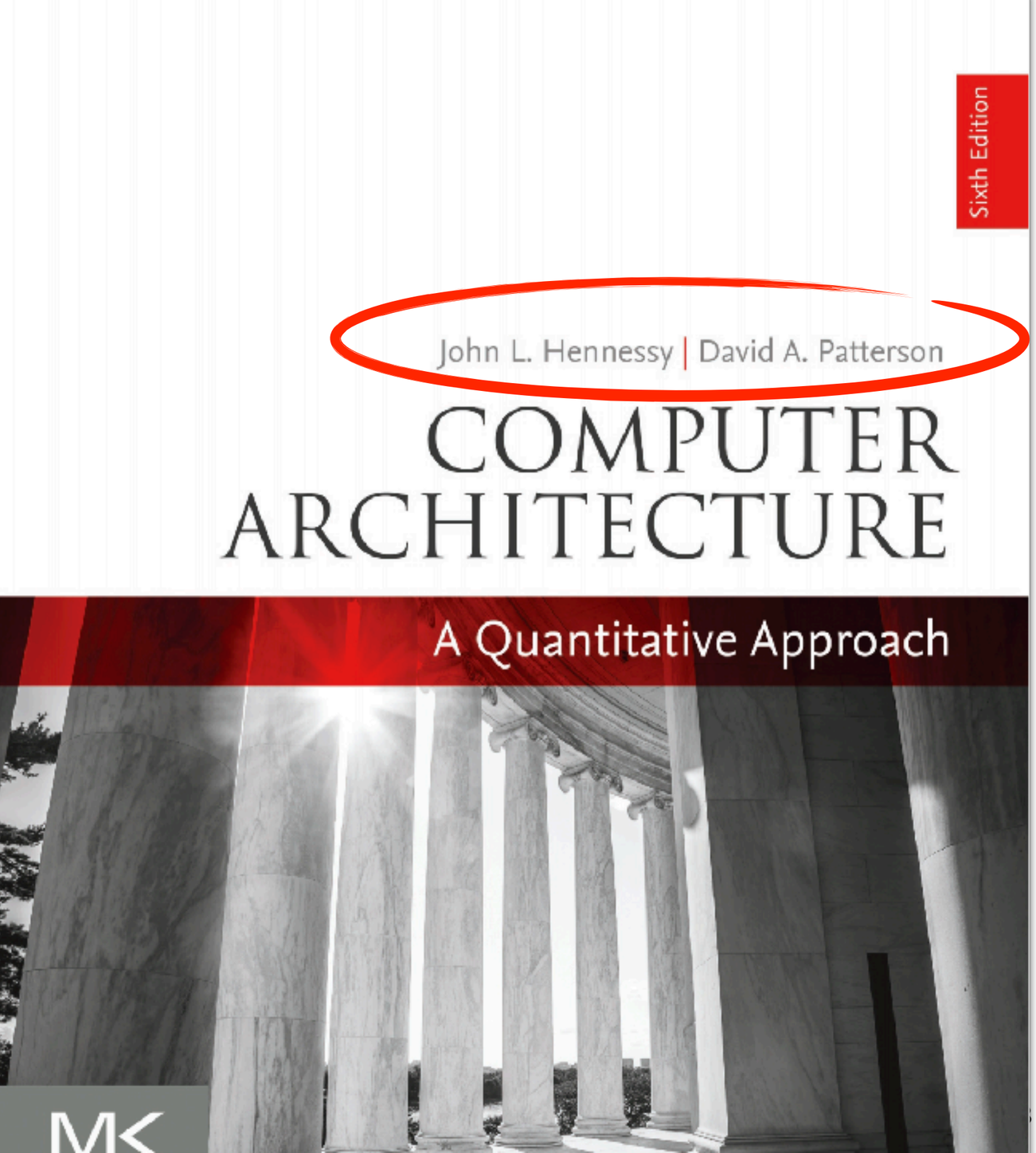
June 23, 2019

5:15pm MST

ACM TURING AWARD since 1966

Geoffrey Hinton

Yann LeCun



Computer Architecture

Enables

Deep Learning

2018 Turing Award

Computer architecture also enables ...

Then, what is“Computer Architecture” really about?

What's computer architecture?

architecture noun

ar·chi·tec·ture | \ ˈär-kə-ˌtek-chər \

Definition of *architecture*

1 : the art or science of building

specifically : the art or practice of designing and constructing habitable ones

2 a : formation or construction resulting from organization
// the *architecture* of the garden

b : a unifying or coherent form or structure
// a novel that lacks *architecture*

3 : architectural product or work
// buildings that comprise the *architecture* of the square

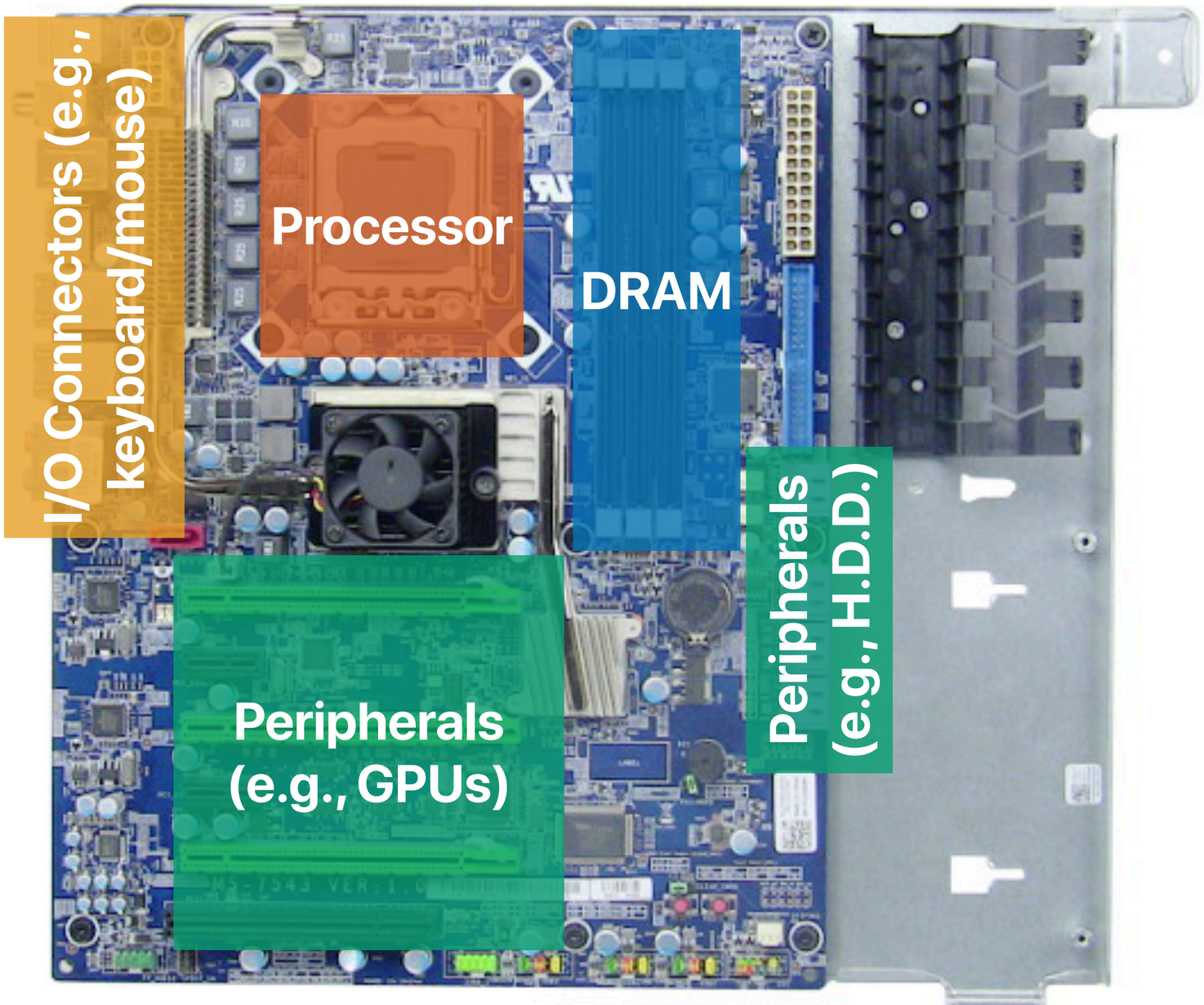
4 : a method or style of building
// Gothic *architecture*

5 : the manner in which the components of a computer or computer system are organized and integrated
// different program *architectures*

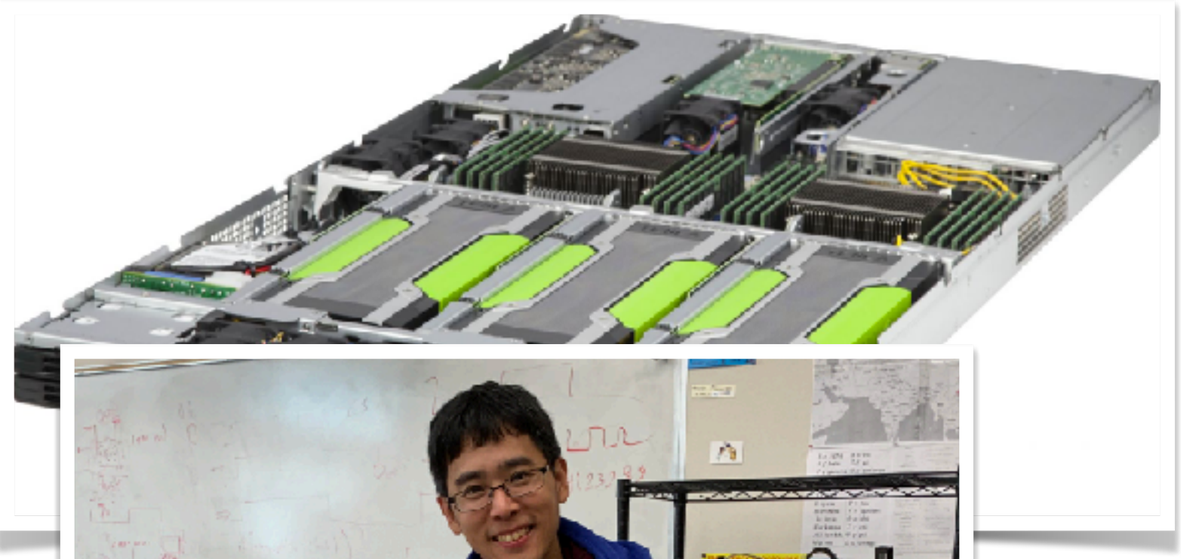
The manner in which the components of a computer or computer system are organized and integrated

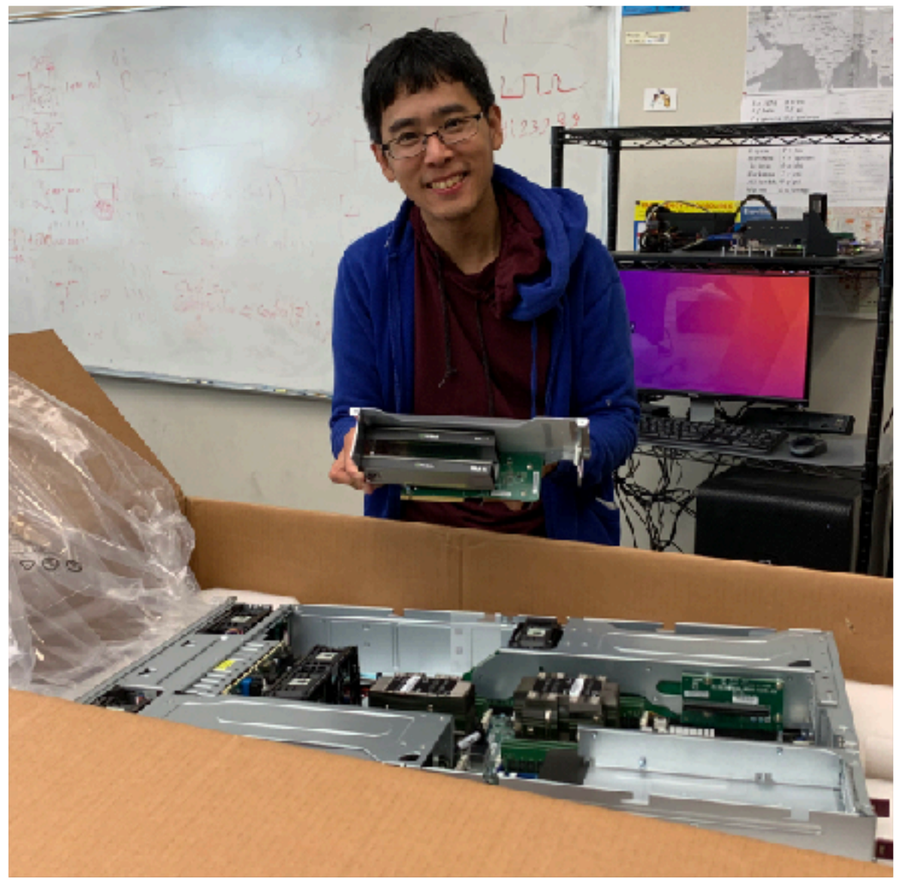
What're those "components"?

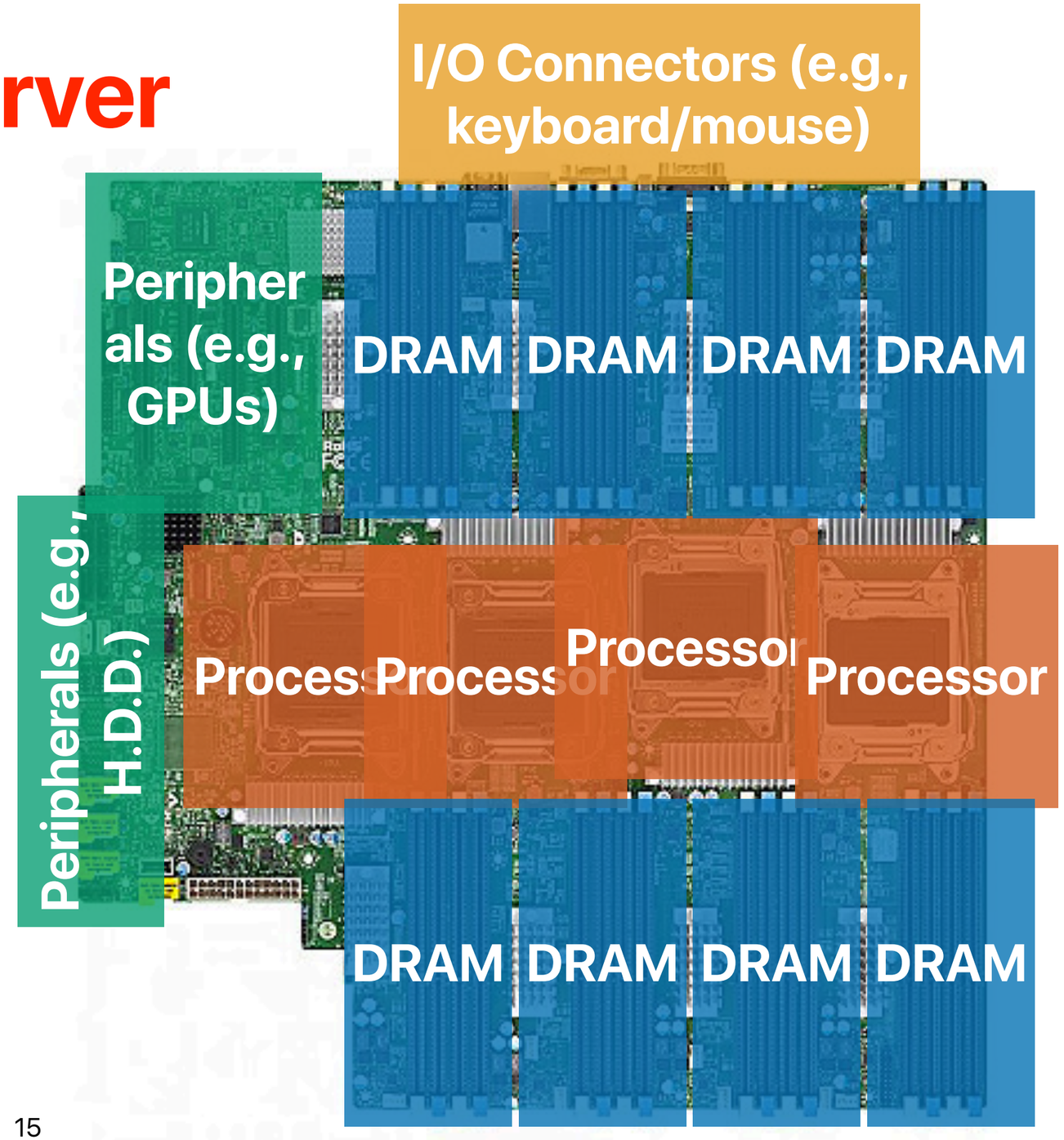
Desktop Computer



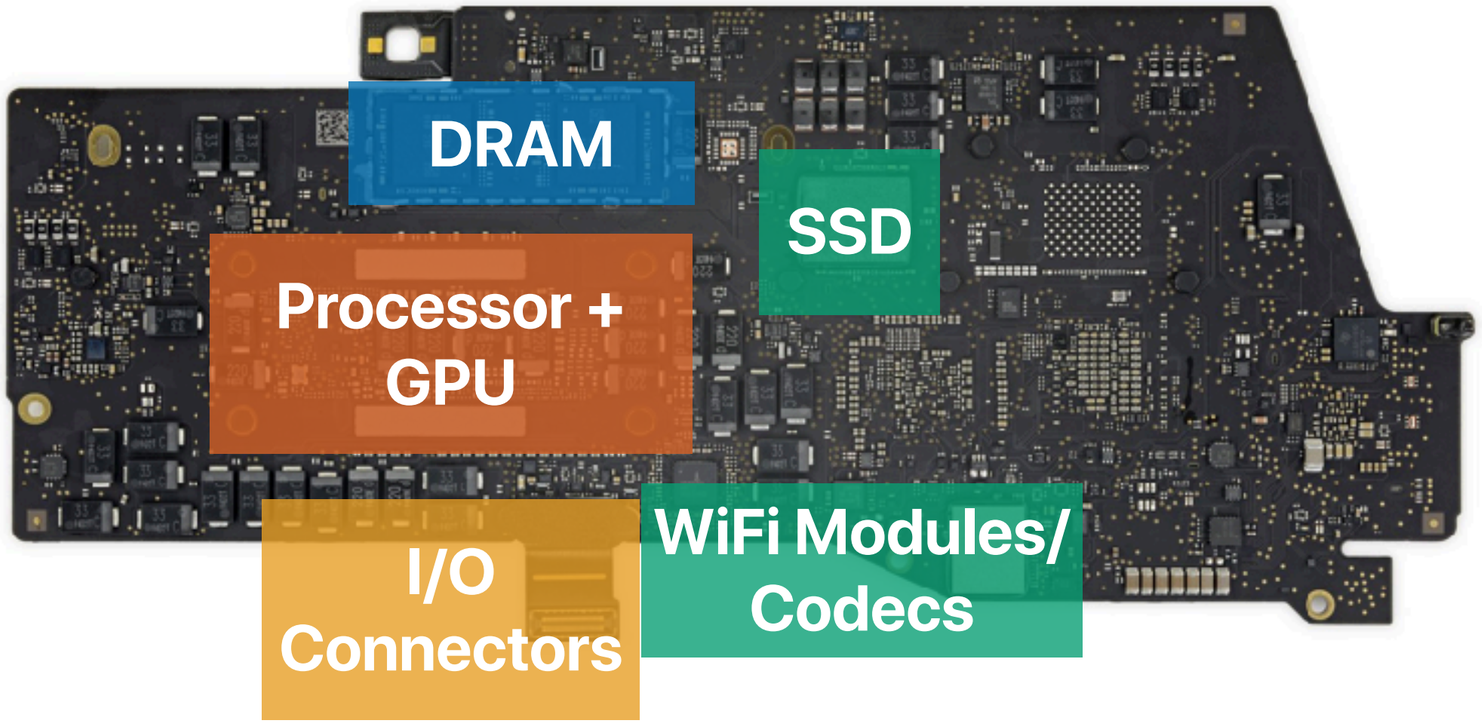
Server



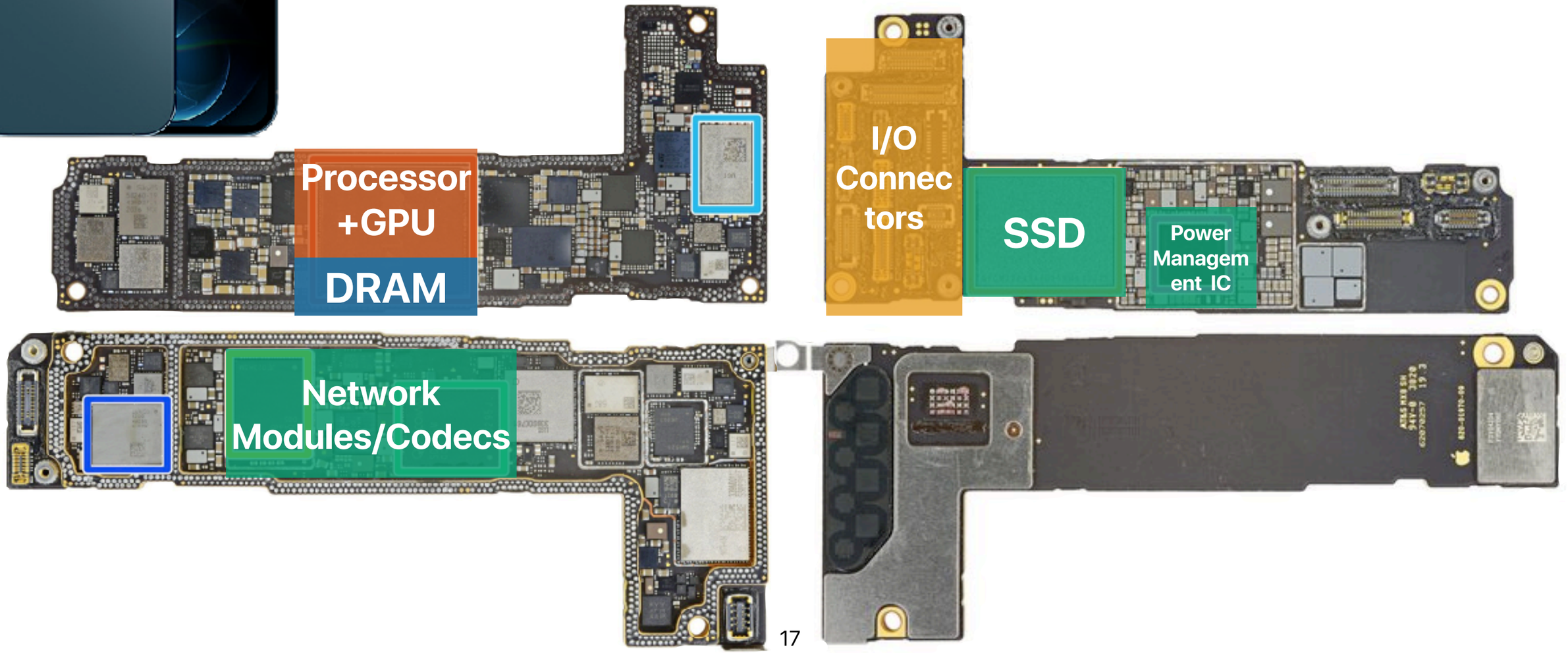



I/O Connectors (e.g., keyboard/mouse)
Peripherals (e.g., GPUs)
DRAM
DRAM
DRAM
DRAM
Peripherals (e.g., H.D.D.)
Processor
Processor
Processor
Processor
DRAM
DRAM
DRAM
DRAM

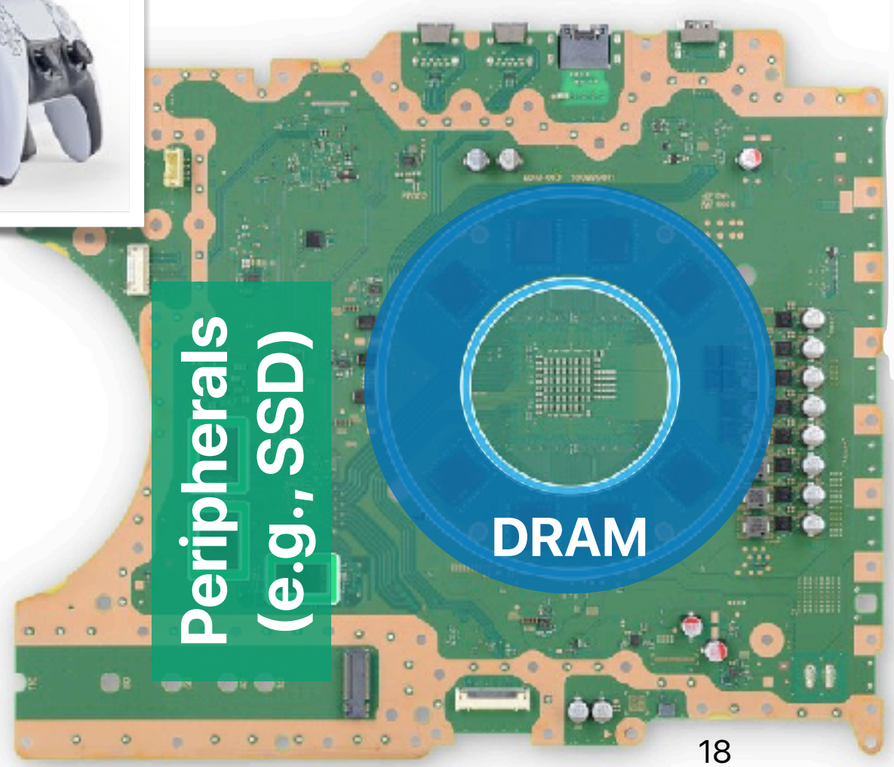
MacBook Pro 13″

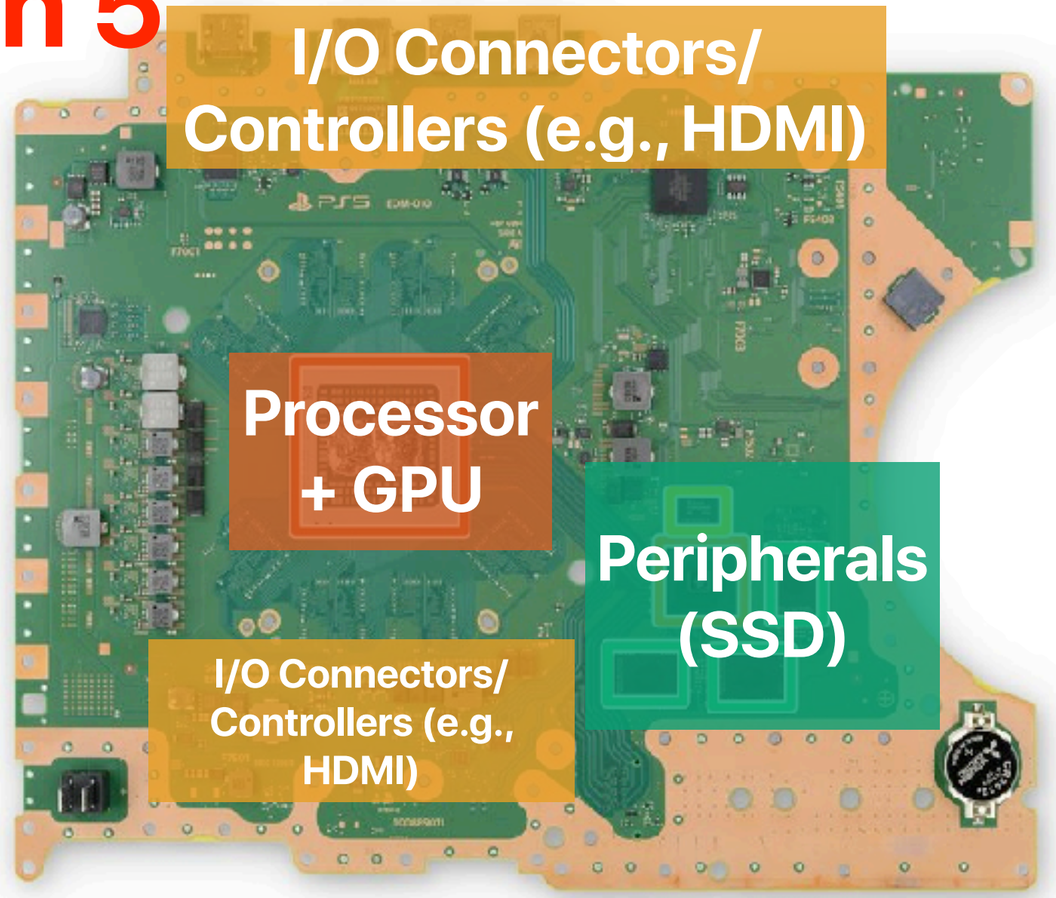


iPhone 12 Pro

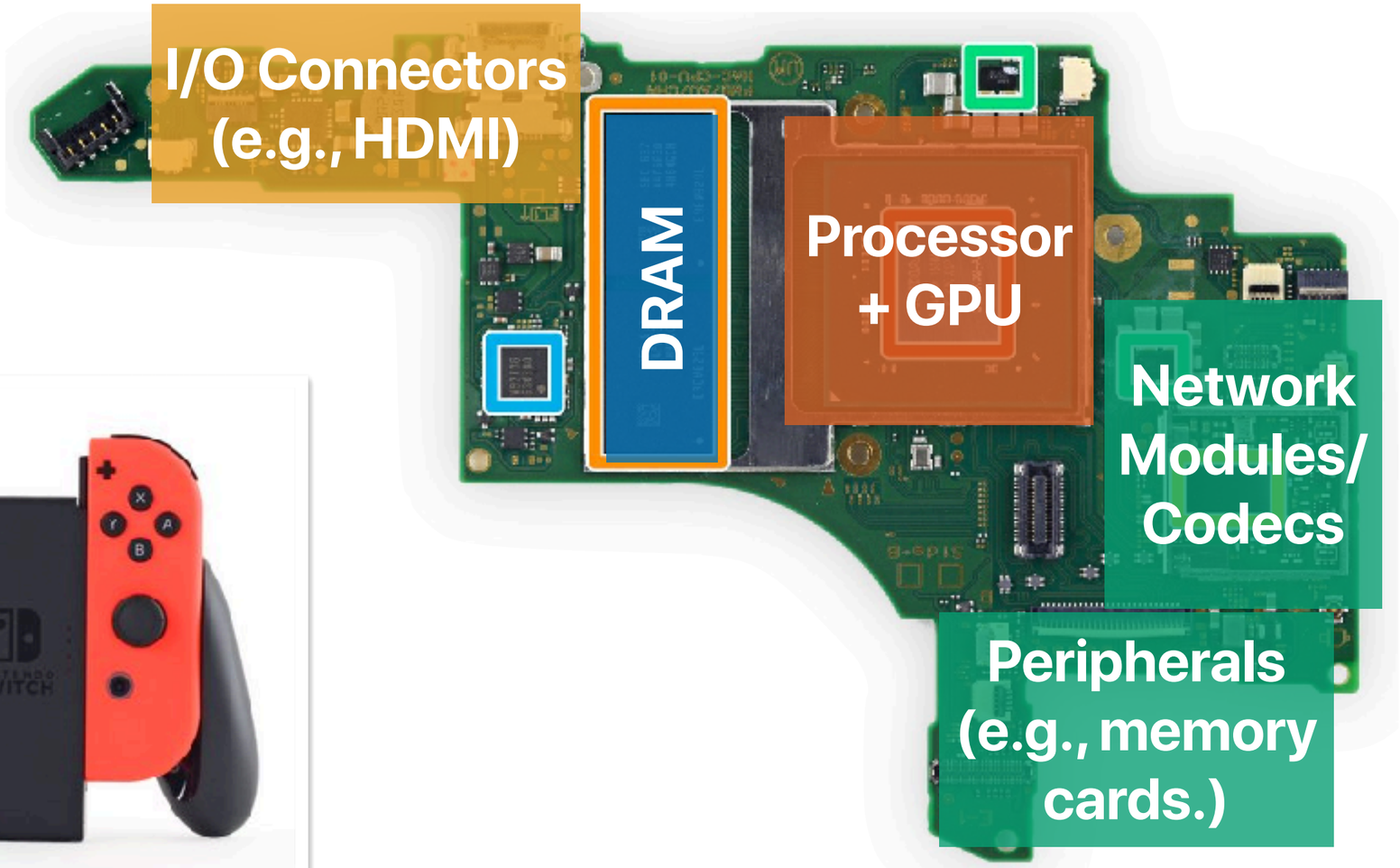


Play Station 5

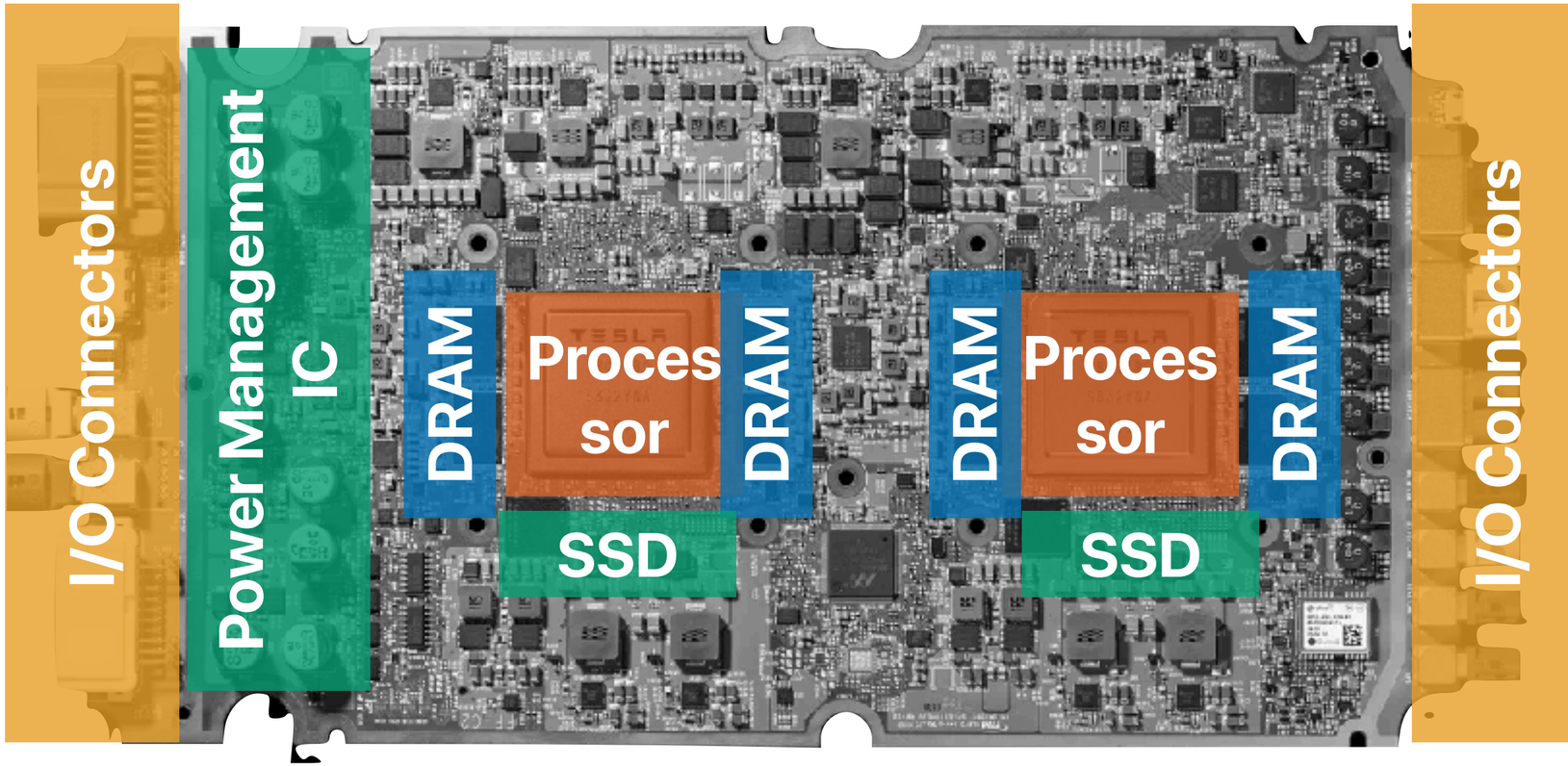




Nintendo Switch

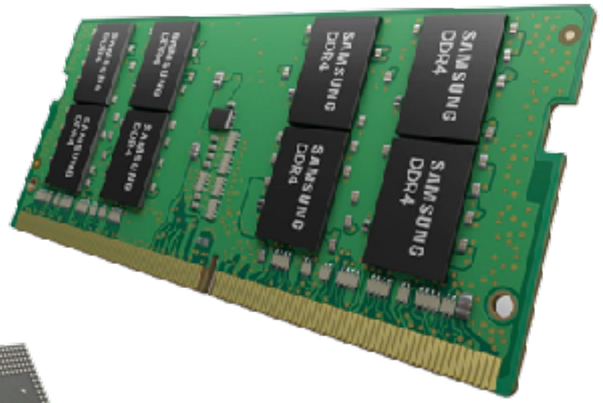


Tesla Model 3



Processors and memory modules are everywhere!

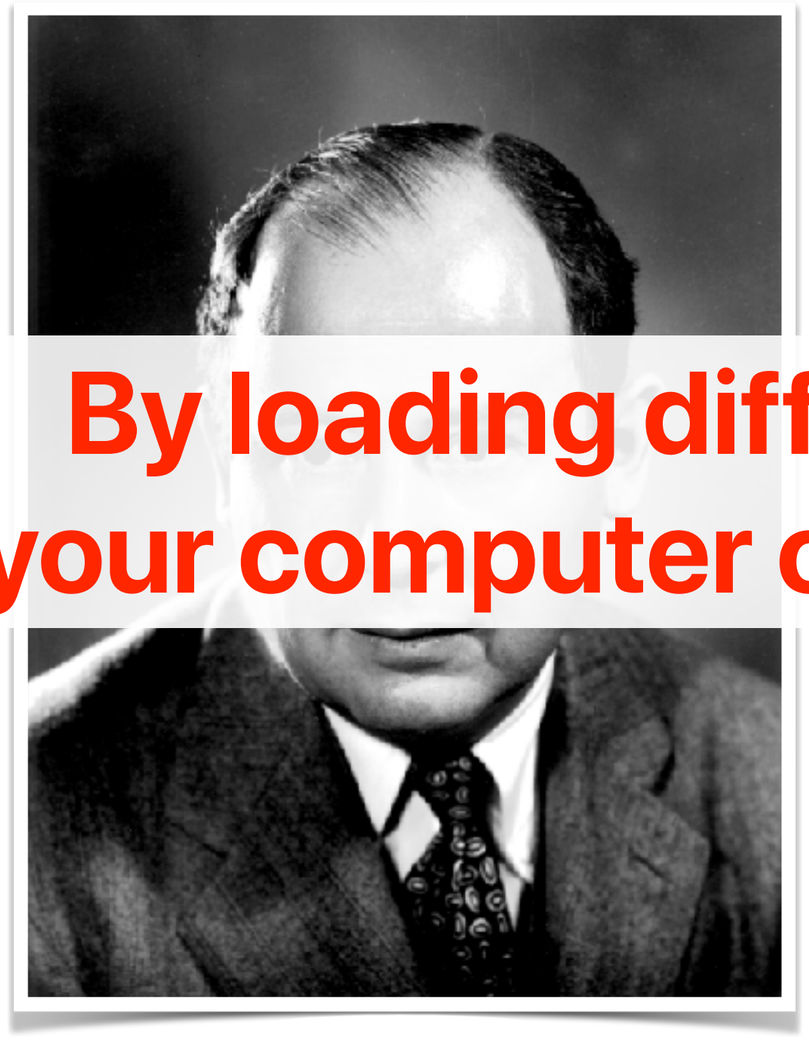
Processors



Memory

Why are “Processor” & “Memory” everywhere?

von Neumman Architecture



509cbd23

00c2e800

Processor

By loading different programs into memory, your computer can perform different functions

Instruction

130020e4
00003d24
2ca4e2b3

Data

00c30000
00000008

Memory

Program

Instruction

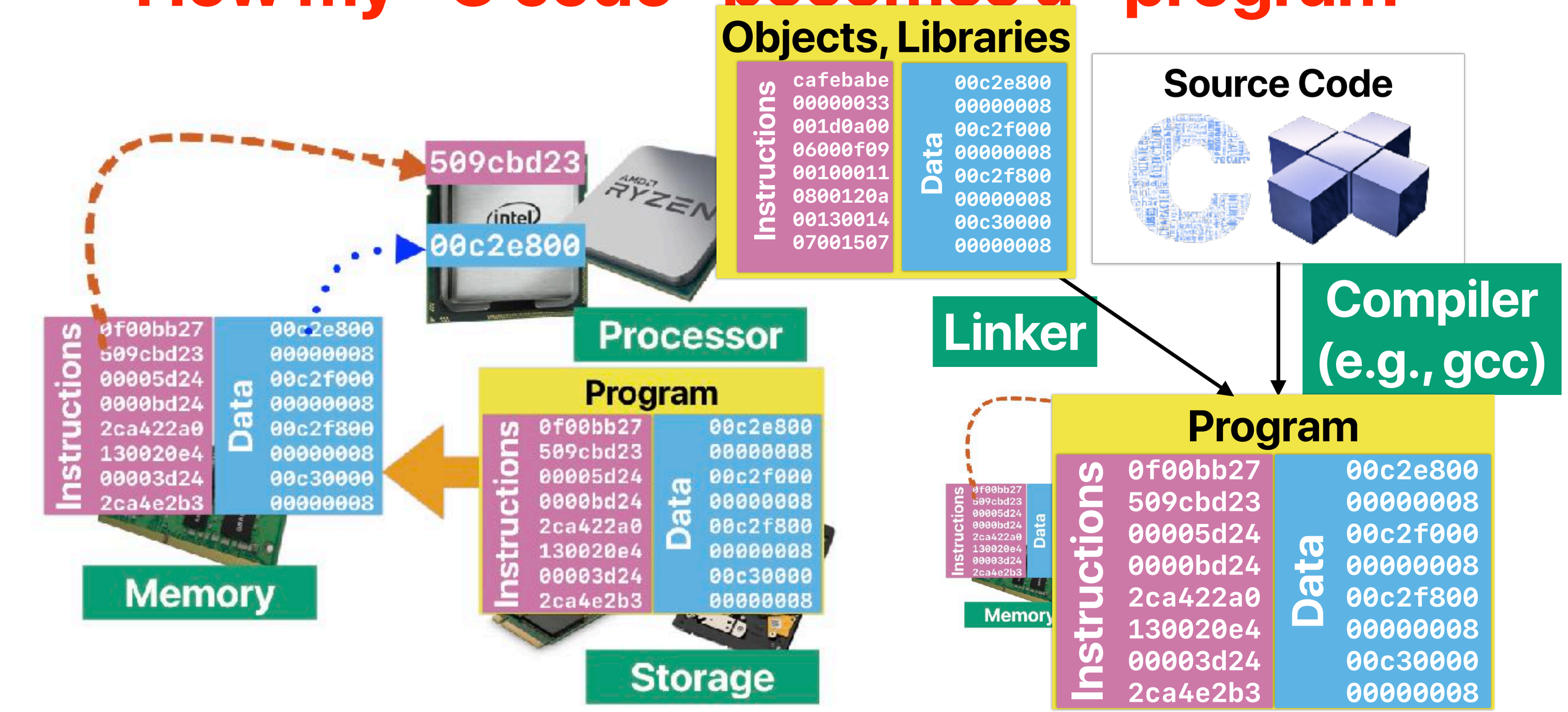
509cbd23
00005d24
0000bd24
2ca422a0
130020e4
00003d24
2ca4e2b3

Data

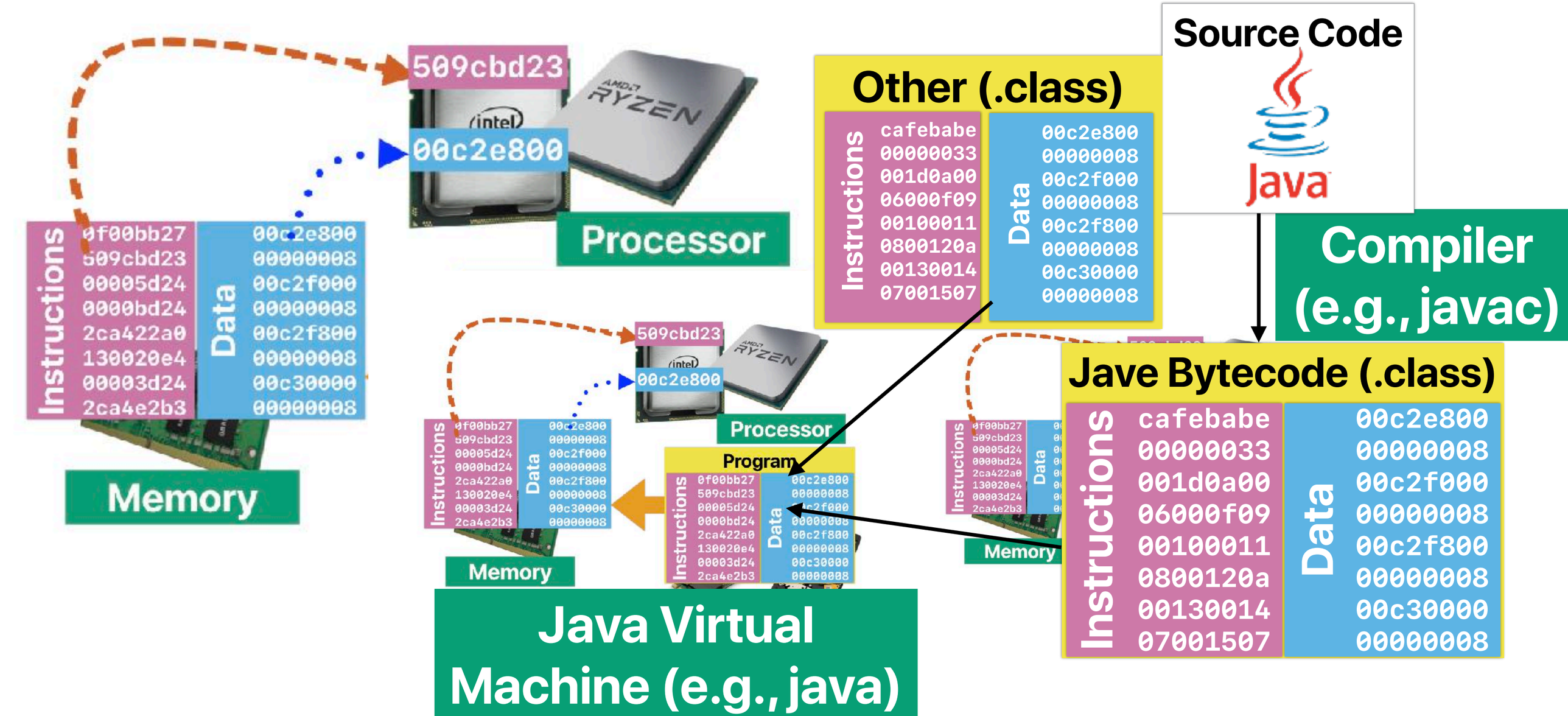
00000008
00c2f000
00000008
00c2f800
00000008
00c30000
00000008

Storage

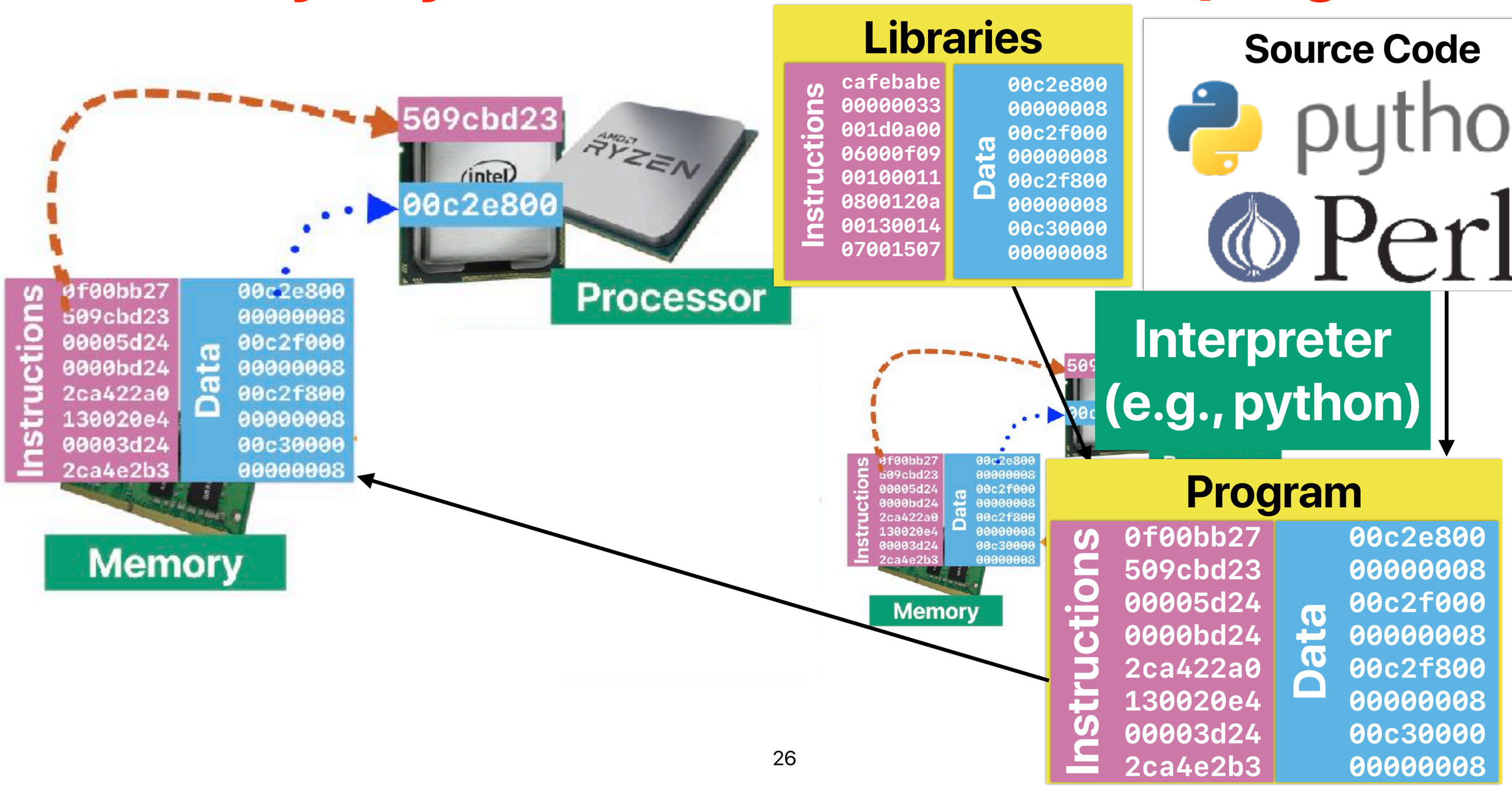
How my "C code" becomes a "program"



How my “Java code” becomes a “program”

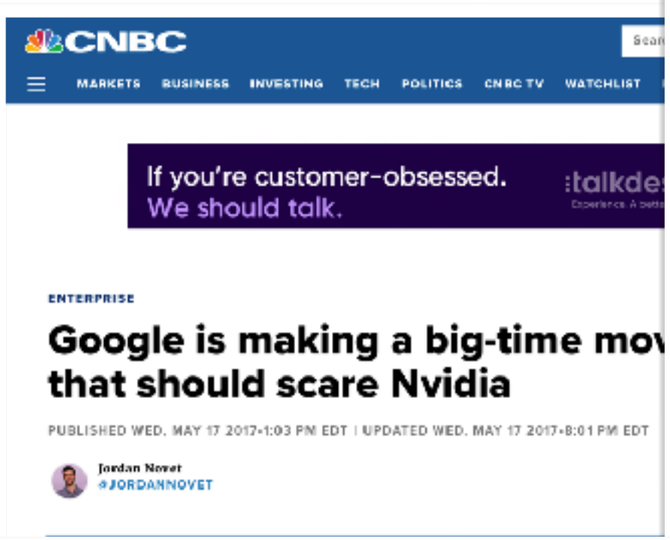


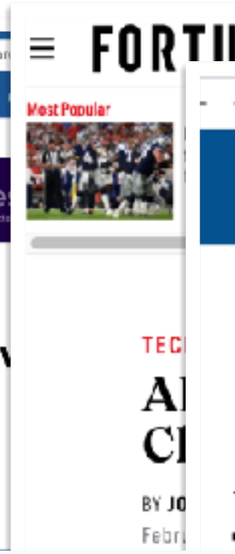
How my "Python code" becomes a "program"

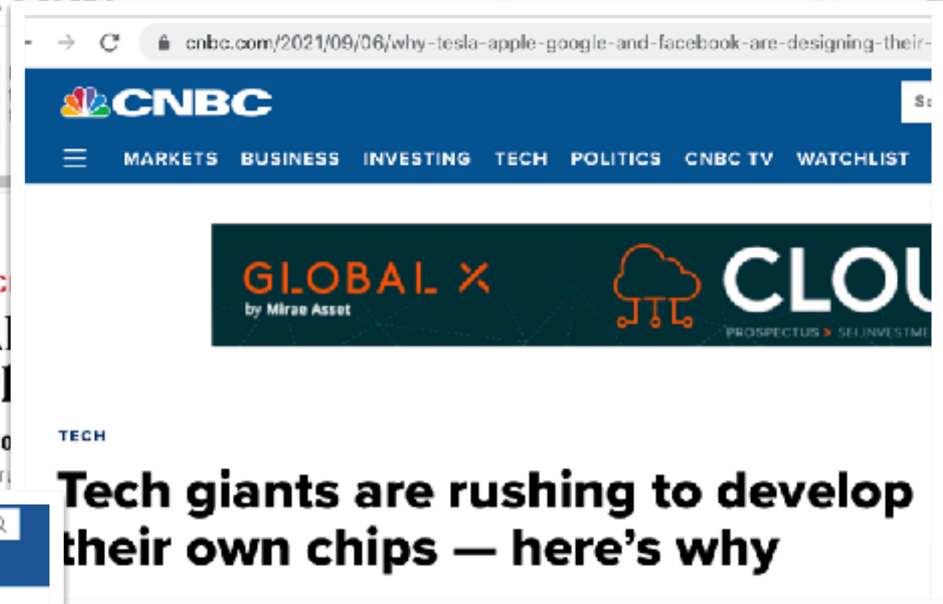


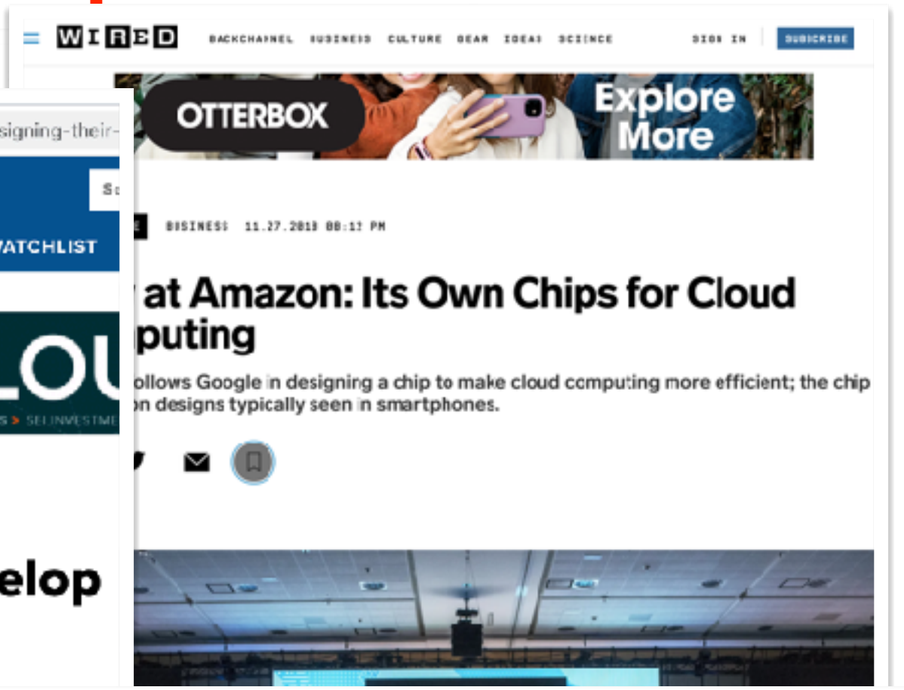
OK, I know computer architecture is important. But will that give me a job?

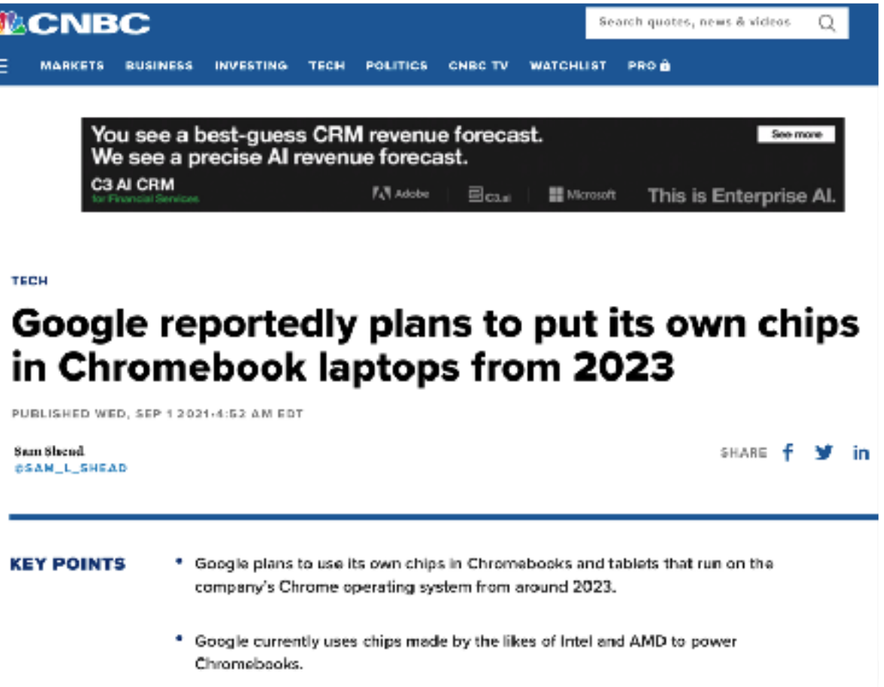
We're now at a "New Golden Age" of computer architecture

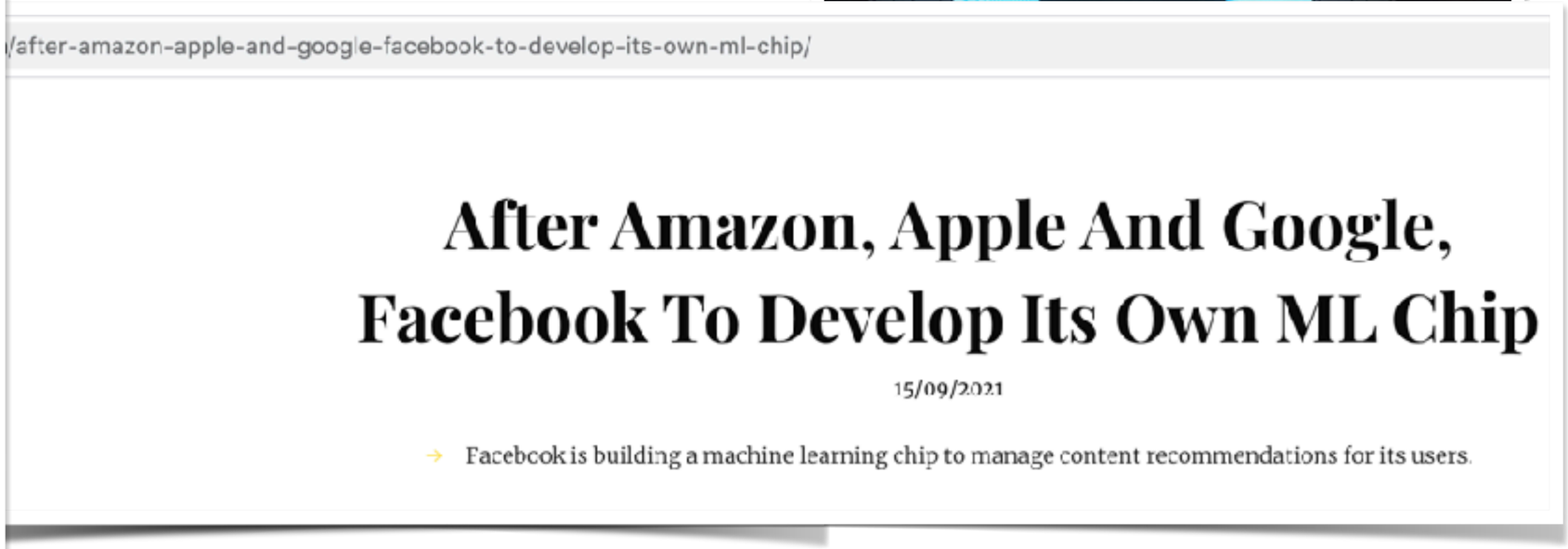












We're now at a "New Golden Age" of computer architecture

Conclusion: A New Golden Age

- End of Dennard Scaling and Moore's Law
  ⇒ architecture innovation to improve performance/cost/energy
- Security ⇒ architecture innovation too
- Domain Specific Languages ⇒ Domain Specific Architectures
- Free, open architectures and open source implementations
  ⇒ everyone can innovate and contribute
- Cloud FPGAs ⇒ all can design and deploy custom "HW"
- Agile HW development ⇒ all can afford to make (small) chips
- Like 1980s, great time for architects in academia & in industry!

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Challenges of von Neumann Architecture

Moore's Law[1]

Present and future

By integrated electronics, I mean
technologies which are referred to
tronics today as well as any additi
result in electronics functions suppli
to miniaturize electronics equipment
creasingly complex electronic functi
space with minimum weight. Sever
evolved, including microassembly
individual components, thin-film
semiconductor integrated circuits.

ICs are increasingly p

The establishment

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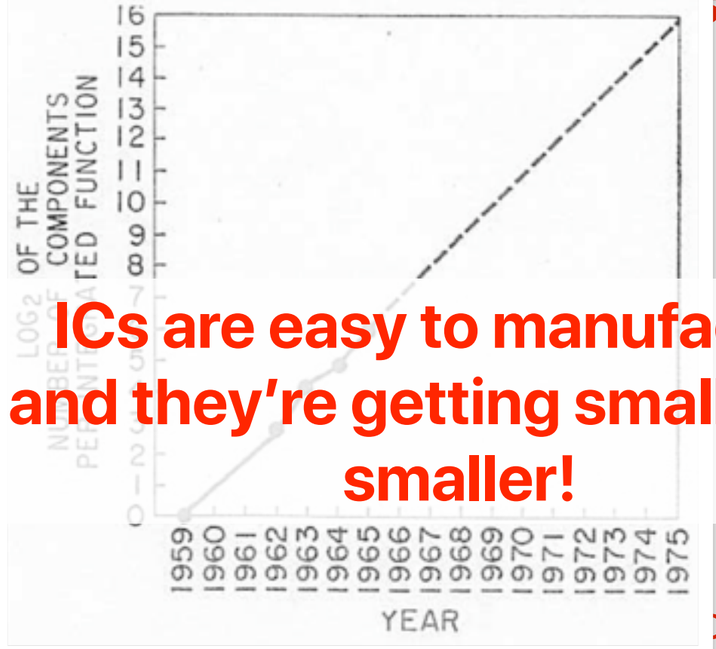
stablish

Increasing the yield

There is no fundamental obstacle to achieving device yields of 100%. At present, packaging costs so far exceed the cost of the semiconductor structure itself that there is no incentive to improve yields, but they can be raised as high as is economically justified. No barrier exists comparable to the thermodynamic equilibrium considerations



ICs are easy to manufacture and they're getting smaller and smaller!

Two-mil squares

With the dimensional tolerances already being
employed in integrated circuits, isolated high-per
formance transistors can be built on centers two
thousandths of an inch apart. Such a two-mil square
can also contain several kilohms of resistance o

ICs are small

Linear circuitry

Integration will not change linear systems as radically as digital systems. Still, a considerable degree of integration will be achieved with linear

ICs are widely applicable

Reliability coun

In almost e
demonstrated h
level of production—low compared to that of discrete components—it offers reduced systems cost, and in many systems improved performance has been realized.

ICs are more reliable

Heat problem

Will it be possible to remove the heat generated by tens of thousands of components in a single silicon chip?

Heat is a solvable issue

Day of reckoning

Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array. Perhaps newly devised de-

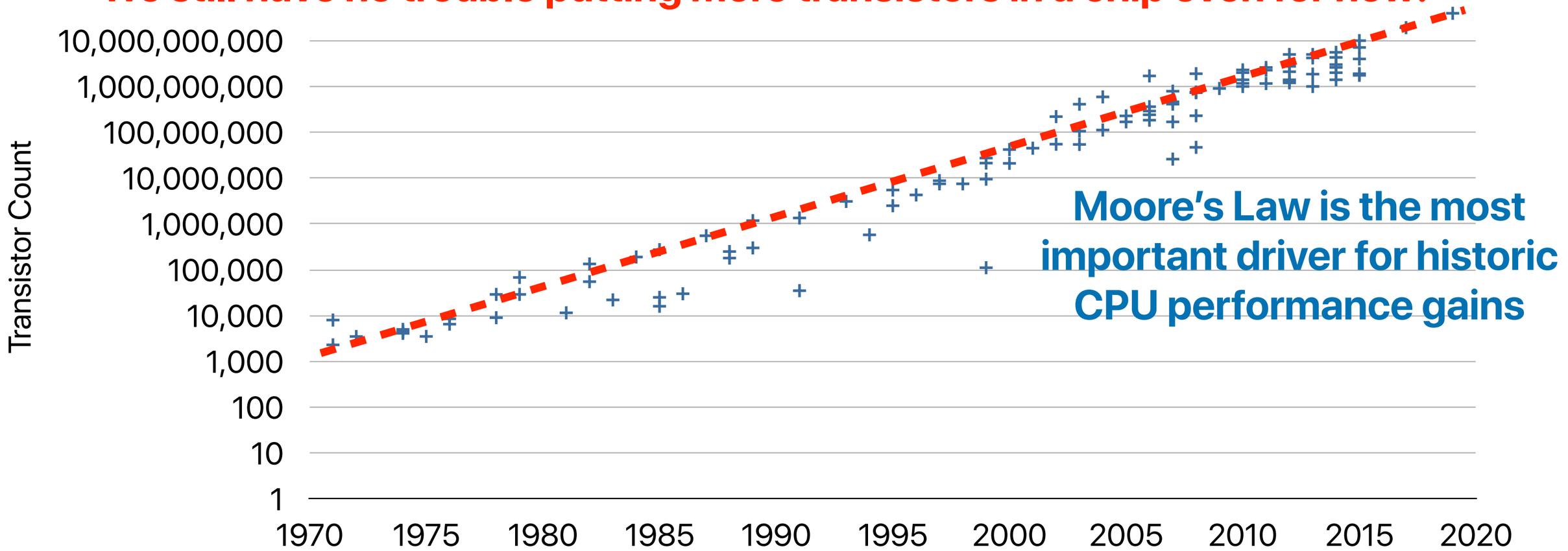
Designing ICs can be easy

(1) Mo mponents onto integrated circuits', Electronics 38 (8) .

Moore's Law[1]

- The number of transistors we can build in a fixed area of silicon doubles every 12 ~ 24 months.

We still have no trouble putting more transistors in a chip even for now!

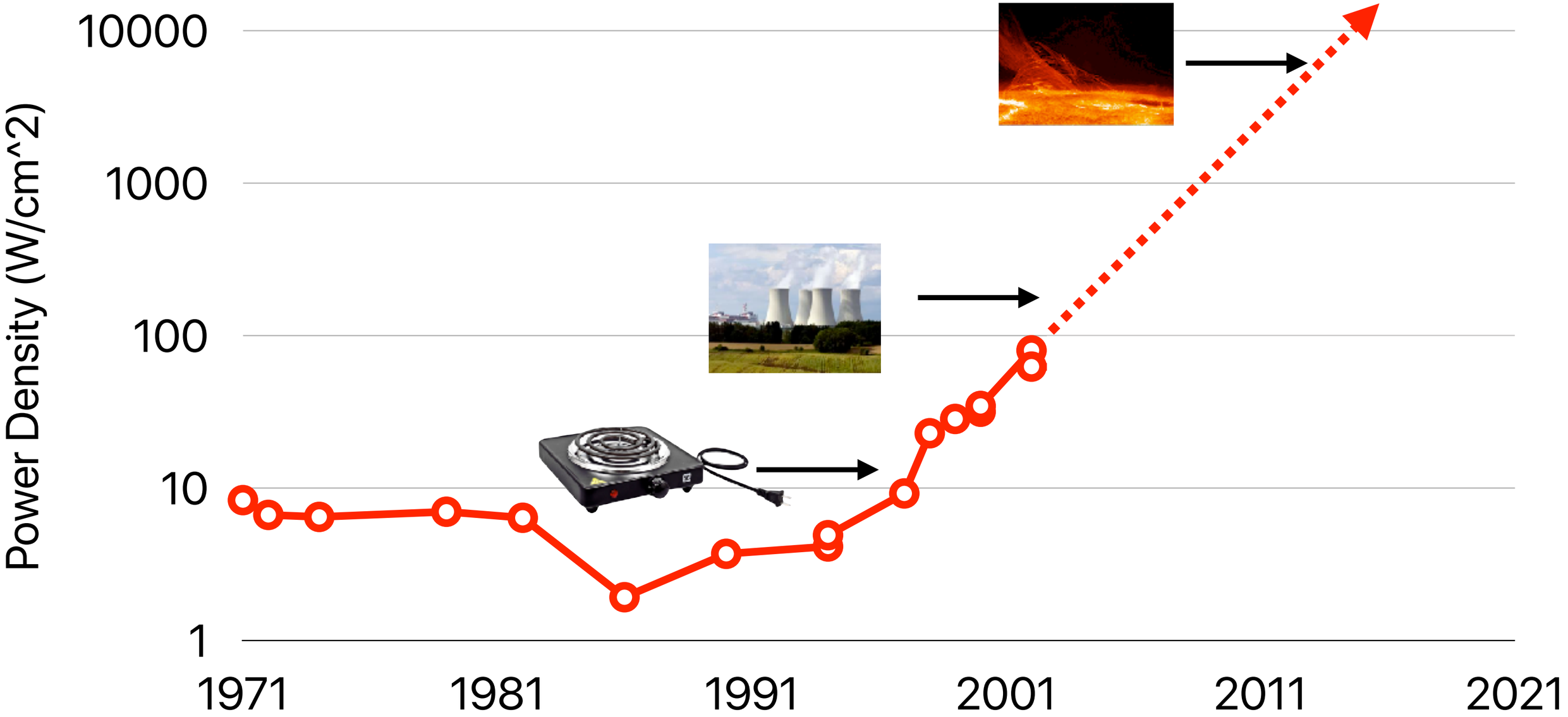


(1) Moore, G. E. (1965), 'Cramming more components onto integrated circuits', Electronics 38 (8) .

Plot based on https://en.wikipedia.org/wiki/Transistor_count by Hung-Wei Tseng

Moore’s Law still alive, but not that useful. Because …

Power Density of Processors



Power consumption & power density

- The power consumption due to the switching of transistor states
- Dynamic power per transistor:

$$P_{dynamic} \sim \alpha \times C \times V^2 \times f \times N$$

  - α: average switches per cycle
  - C: capacitance
  - V: voltage
  - f: frequency, usually linear with V
  - N: the number of transistors

We cannot make chips always operating at very high frequencies

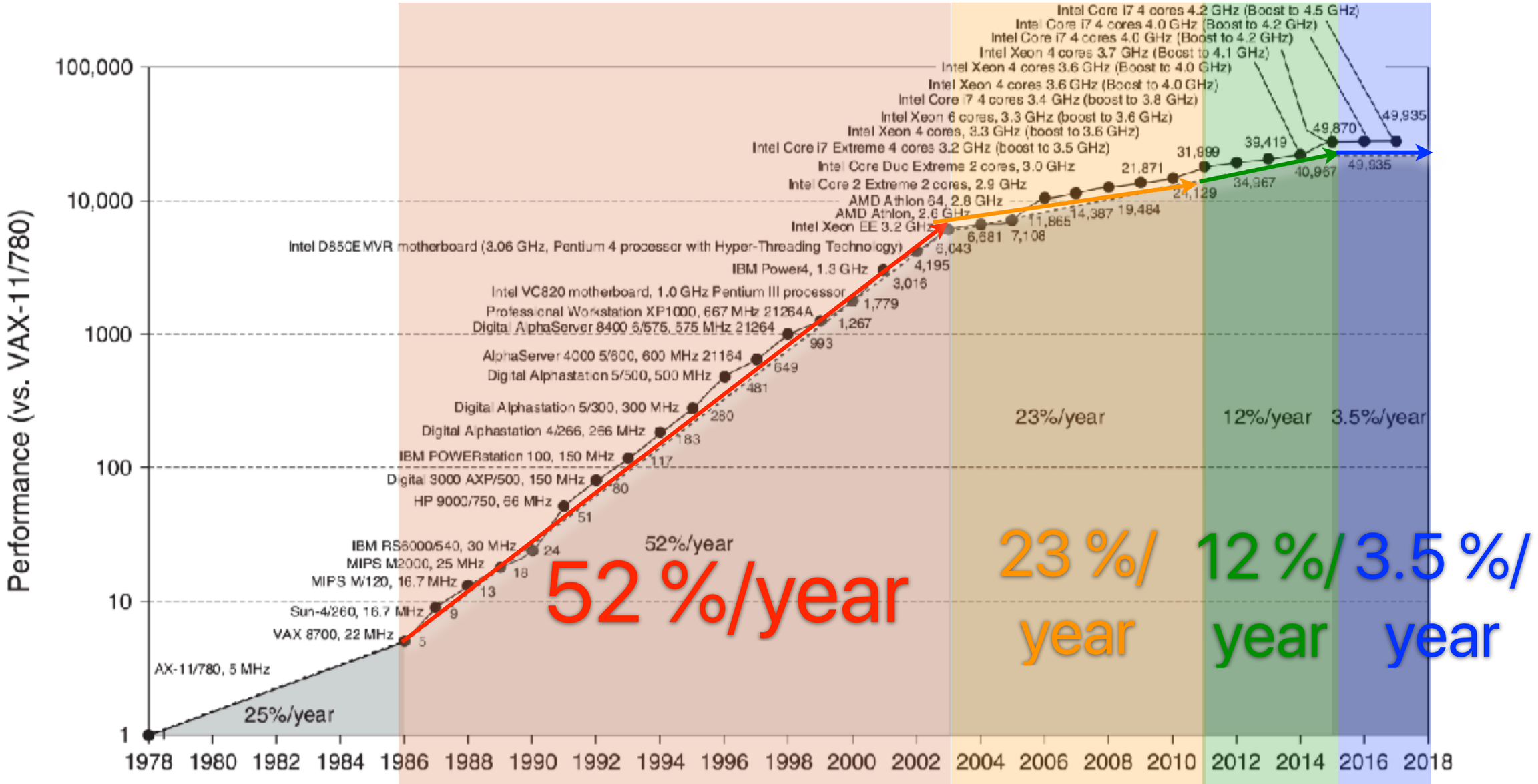
- Power density:

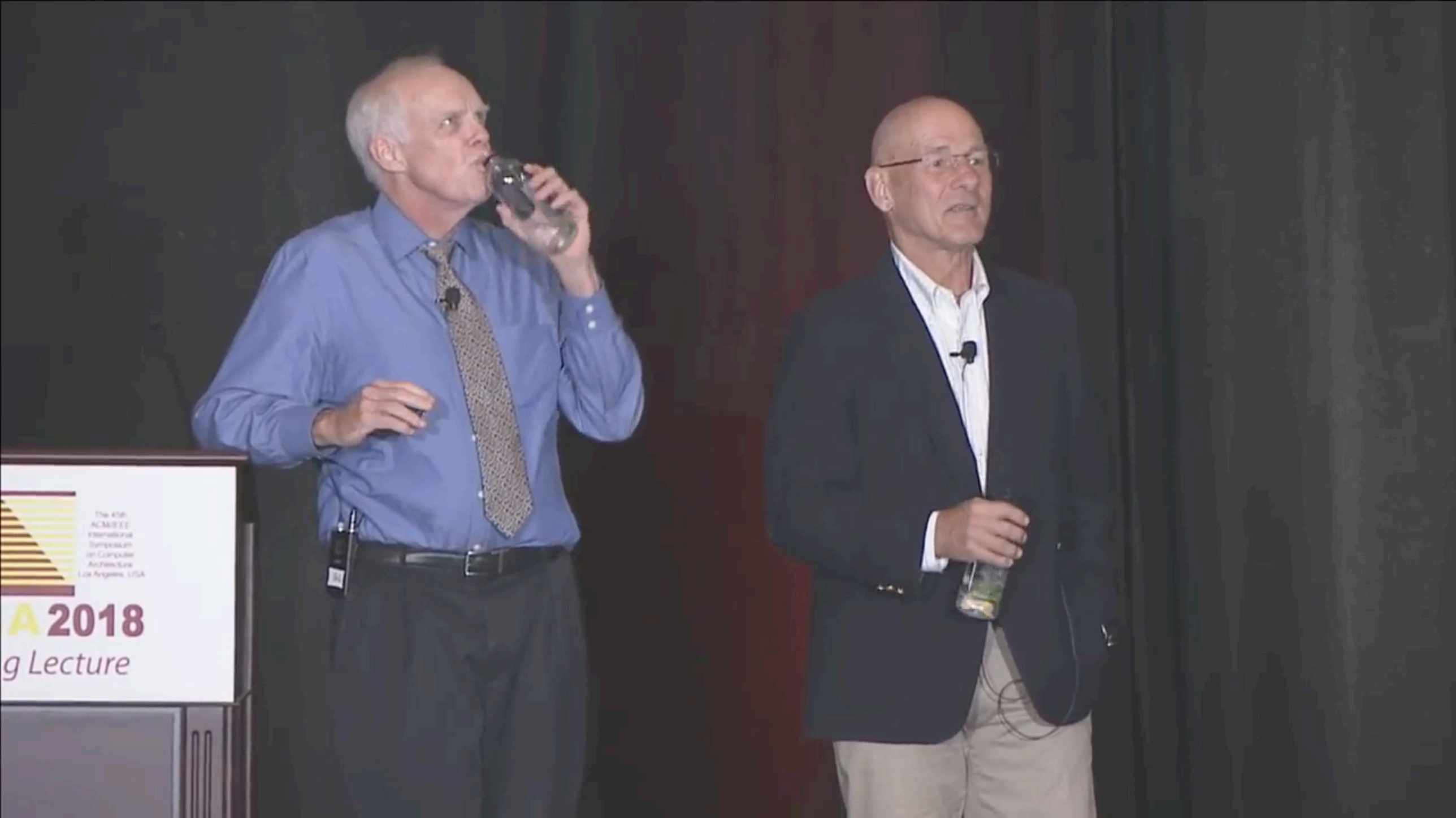
$$P_{density} = \frac{P}{area}$$

Moore's Law allows higher frequencies as transistors are smaller

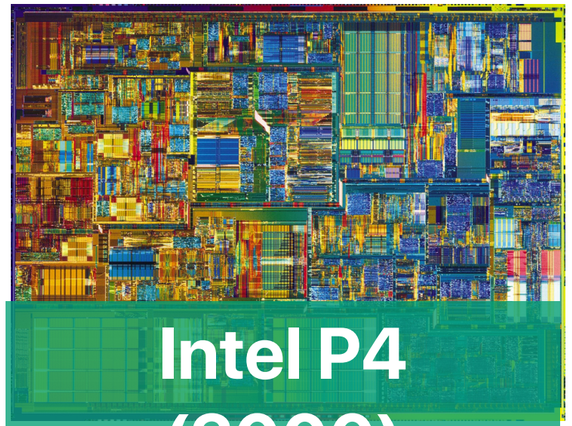
Moore's Law makes this smaller

CPU is important but...

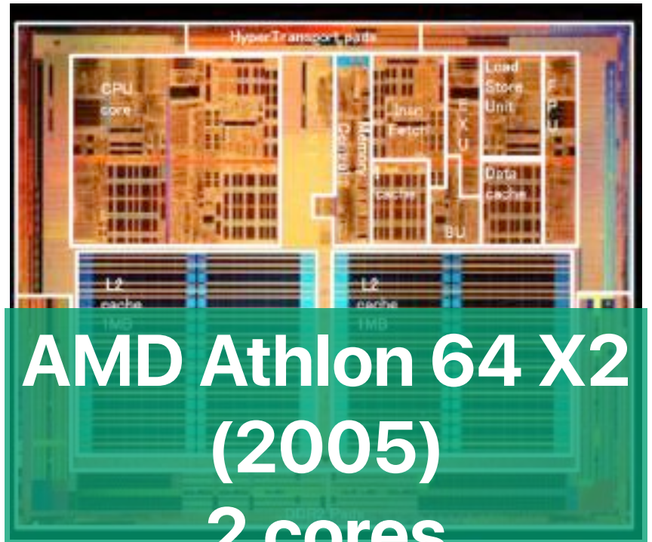



The 45th
ACM/IEEE
International
Symposium
on Computer
Architecture
Los Angeles, USA
A 2018
g Lecture

Multicore processors

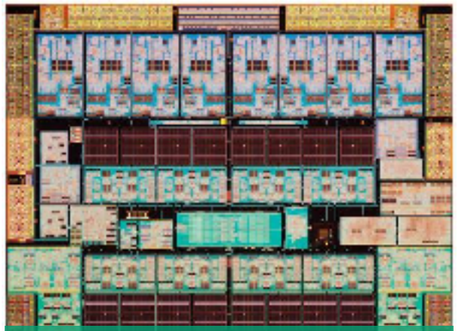


Intel P4
(2000)
1 core

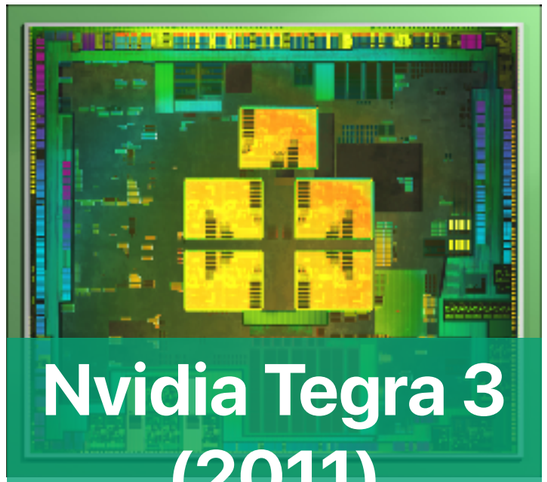


AMD Athlon 64 X2
(2005)
2 cores

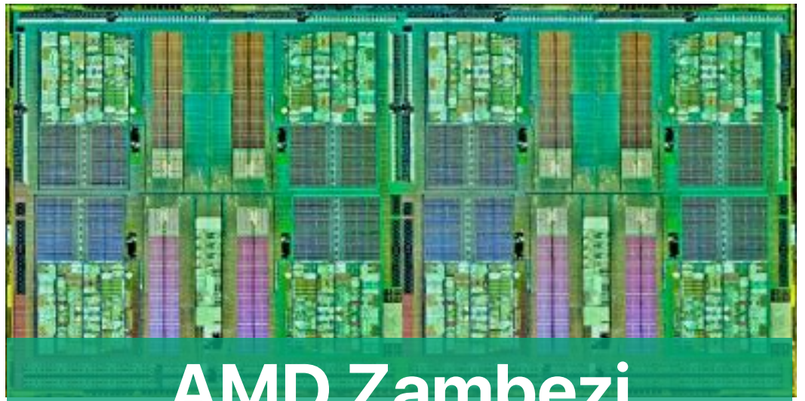
Intel Nahalem
(2010)
4 cores



SPARC T3
(2010)
16 cores

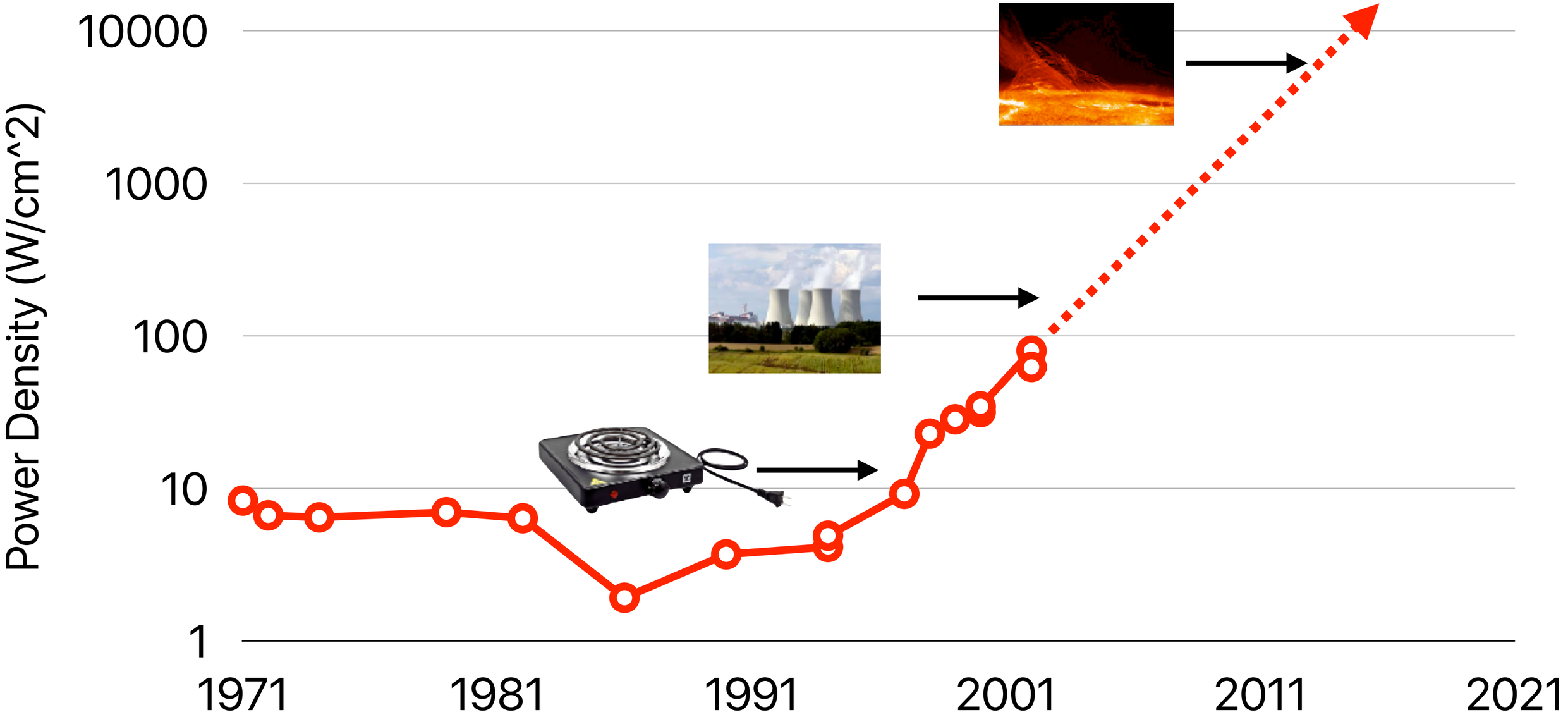


Nvidia Tegra 3
(2011)
5 cores



AMD Zambezi
(2011)
16 cores

Power Density of Processors



Dennardian Broken

- Given a scaling factor S

Parameter	Relation	Classical Scaling	Leakage Limited
Power Budget		1	1
Chip Size		1	1
Vdd (Supply Voltage)		1/S	1
Vt (Threshold Voltage)	1/S	1/S	1
tex (oxide thickness)		1/S	1/S
W, L (transistor		1/S	1/S
Cgate (gate capacitance)	WL/tox	1/S	1/S
Isat (saturation current)	WVdd/tox	1/S	1
F (device frequency)	Isat/(CgateVdd)	S	S
D (Device/Area)	1/(WL)	S^2	S^2
p (device power)	IsatVdd	$1/S^2$	1
P (chip power)	Dp	1	S^2
U (utilization)	1/P	1	$1/S^2$

Static/Leakage Power

- The power consumption due to leakage — transistors do not turn all the way off during no operation
- Becomes the **dominant** factor in the most advanced process technologies.

$$P_{leakage} \sim N \times V \times e^{-V_t}$$

  - N: number of transistors
  - V: voltage
  - V_t: threshold voltage where transistor conducts (begins to switch)

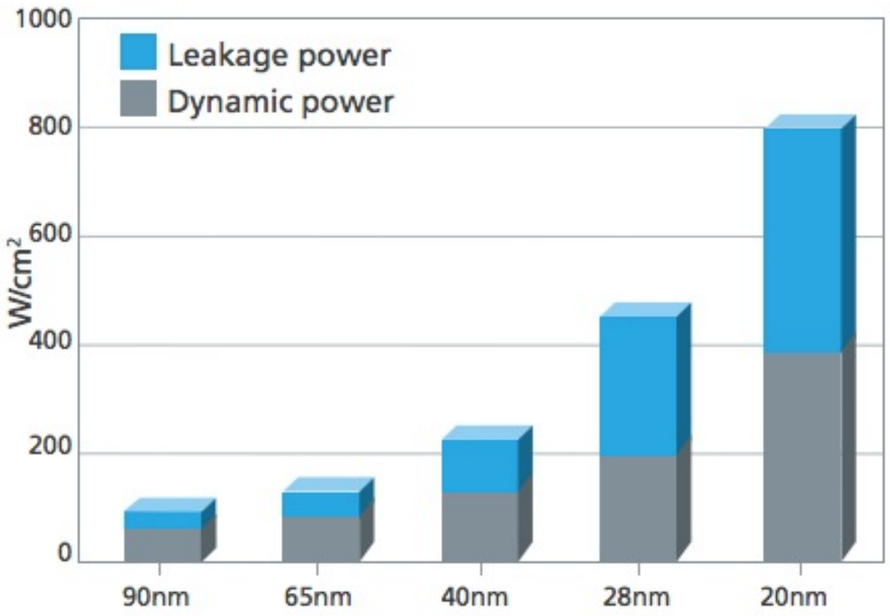


Figure 1: Leakage power becomes a growing problem as demands for more performance and functionality drive chipmakers to nanometer-scale process nodes (Source: IBS).

Power consumption to light on all transistors

Chip

1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1

=49W

Dennardian Scaling

Chip

0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5

=50W

Dennardian Broken

Chip

1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

On ~ 50W

Off ~ 0W

Dark!

=100W!

Los Angeles Times

CALIFORNIA

State of emergency declared as California faces historic heat, possible power outages

A blazing sun silhouettes power lines in North Long Beach ahead of a heatwave that is forecast to begin on Saturday. (Luis Sinco / Los Angeles Times)

By LUKE MONEY | STAFF WRITER

SEP. 4, 2020 | 10:31 AM **UPDATED** 7:35 PM

With potentially historic temperatures set to sear California through Labor Day weekend, Gov. Gavin Newsom issued an emergency proclamation aimed at shoring

CORONAVIRUS AND PANDEMIC ›

Their company got a PPP loan. So why are th still unemployed?

L.A. teachers union opposes opening campus for students with disabilities, English learners

Close-knit Latino family ties bring coronaviru dangers to traditional gatherings

Hair salons can reopen but not malls and sho under new L.A. County plan

Devo's Mark Mothersbaugh nearly died from COVID-19. FaceTiming kept him alive

Cases statewide »

736,248	13,709
confirmed	deaths

As of September 6, 1:38 p.m. Pacific

Dennardian Broken

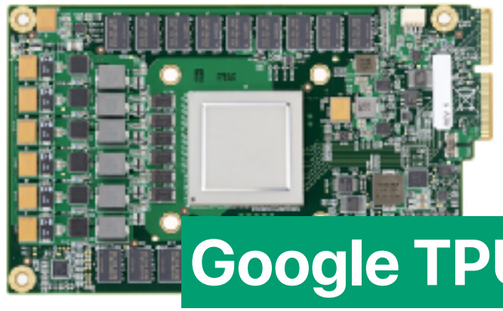
Chip

On ~ 50W

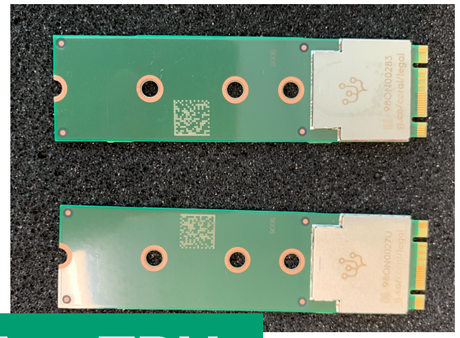
Off ~ 0W

Dark!

The explosion of new AI hardware accelerators



Google TPUv1

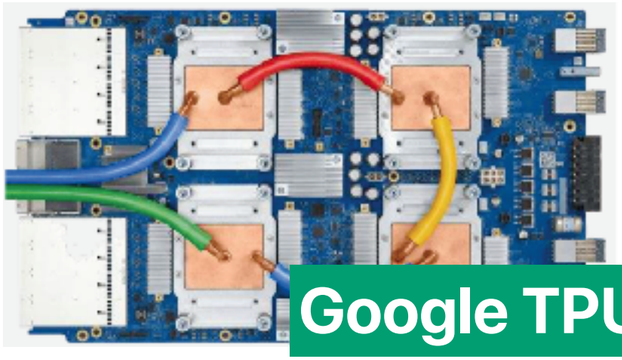


Edge TPUs

Qualcomm Hexagon

Apple Neural Engines

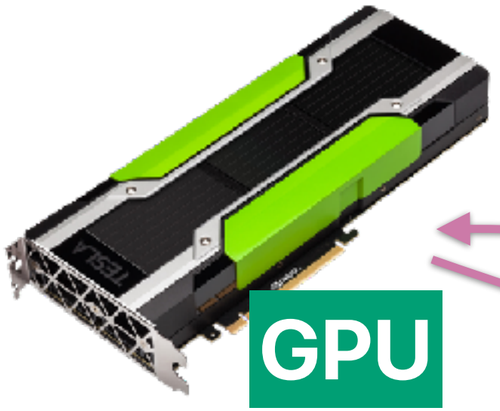
Google TPUv2



Google TPUv3

NVIDIA
Tensor Cores

Heterogeneous Computer Architecture

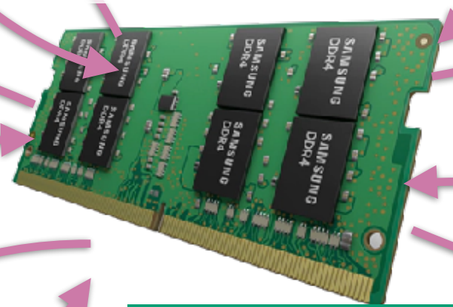


GPU

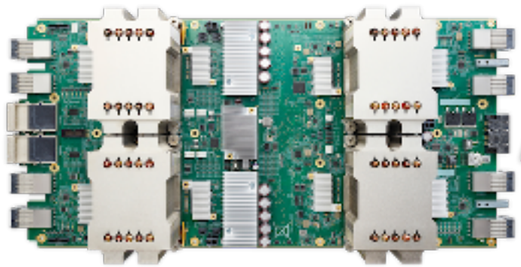
FPGA

Data movements

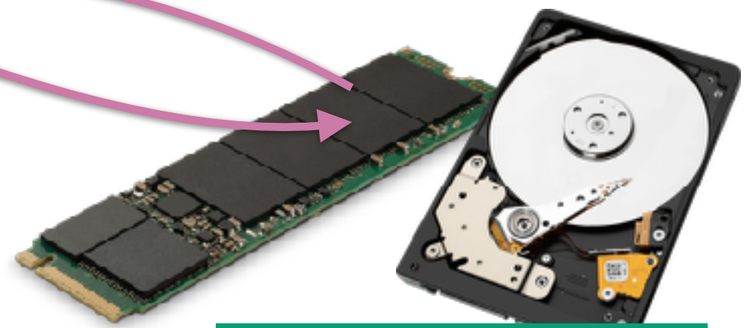
Processor



Memory

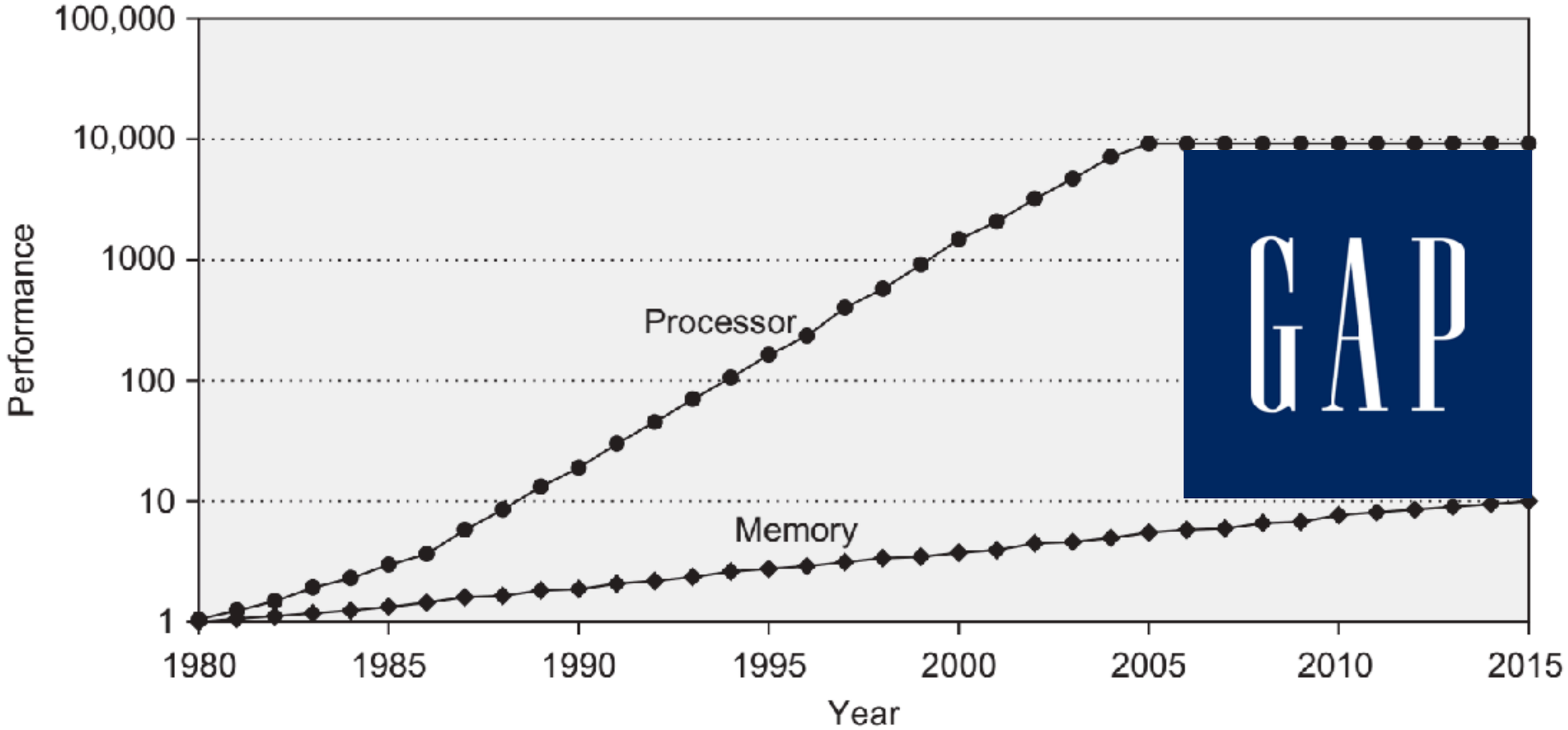


TPU

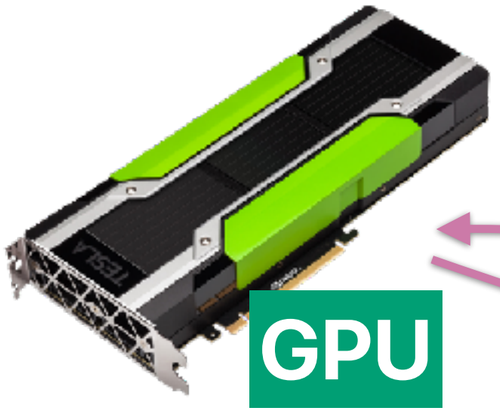


Storage

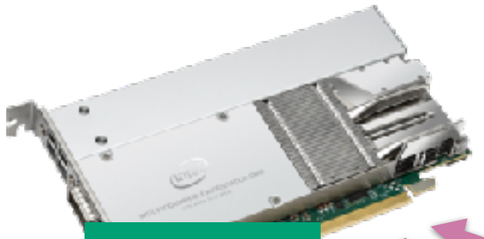
Performance gap between Processor/Memory



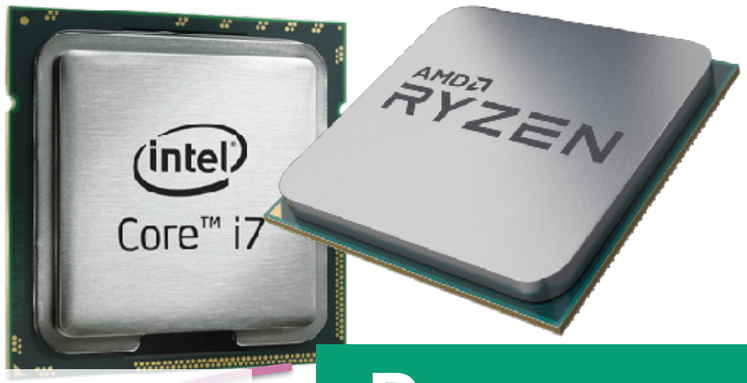
Heterogeneous Computer Architecture



GPU



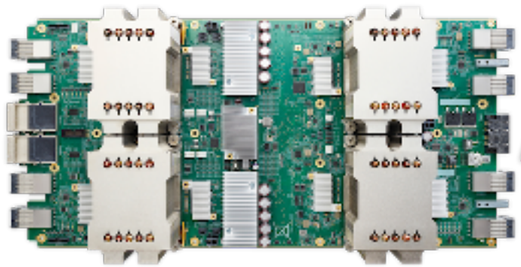
FPGA



Processor

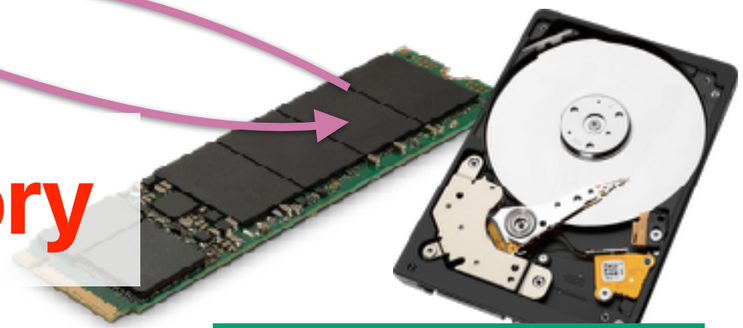
Data movements

Memory



TPU

Slow memory



Storage

I just want to be programmer, so...

What do you care when you're writing a program?

Algorithms
Data Structures
Software Engineering
Computer Architecture
Programming Languages
User Interfaces

Why should I care about “Computer Architecture”

Demo

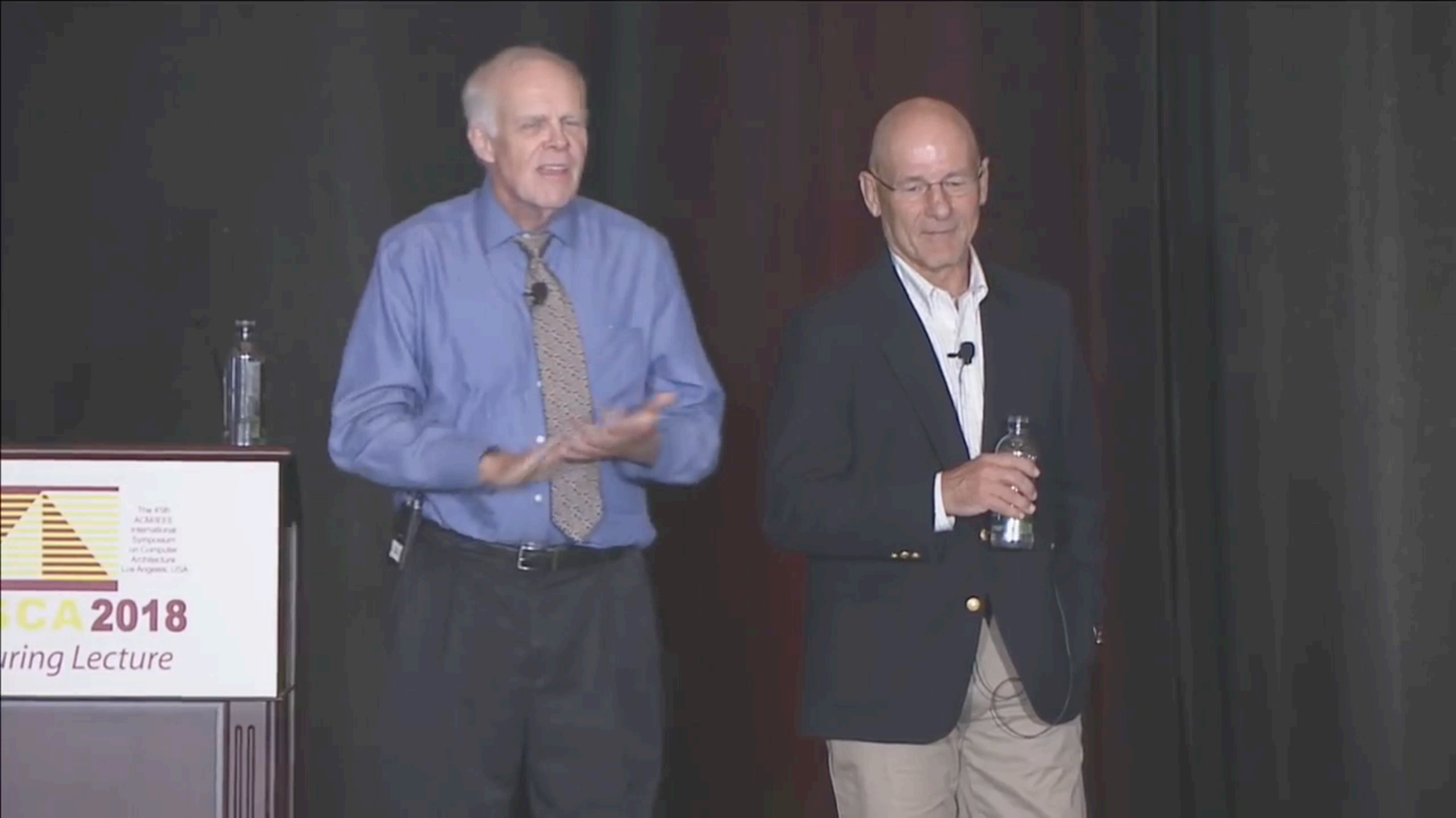
```
if(option)
    std::sort(data, data + arraySize);

for (unsigned c = 0; c < arraySize*1000; ++c) {
        if (data[c%arraySize] >= INT_MAX/2)
            sum ++;
    }
}
```

$O(nlog_2n)$

$O(n)$

if option is set to 1: $O(nlog_2n)$

otherwise, O(n): $O(n)$


The 45th
ACM/IEEE
International
Symposium
on Computer
Architecture
Los Angeles, USA
CA 2018
uring Lecture

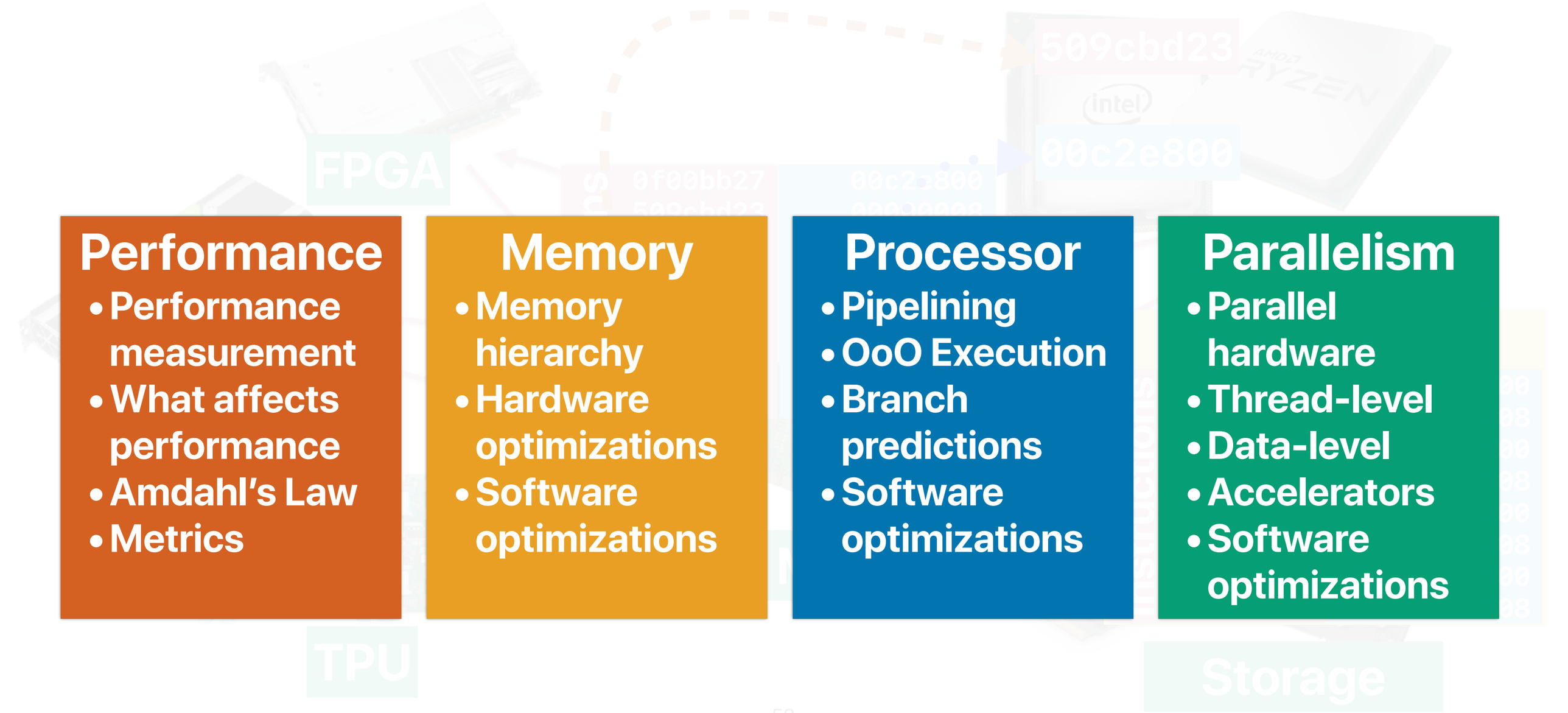
? ? ? ?

Thinking about the washlet

Or a Tesla

What’s going to be in the class?

Heterogeneous Computer Architecture



Performance

- Performance measurement
- What affects performance
- Amdahl's Law
- Metrics

Memory

- Memory hierarchy
- Hardware optimizations
- Software optimizations

Processor

- Pipelining
- OoO Execution
- Branch predictions
- Software optimizations

Parallelism

- Parallel hardware
- Thread-level
- Data-level
- Accelerators
- Software optimizations

Tentative Schedule (on Website)

	Topic	Reading	Slides — Preview	Slides — Release	Due
10/05/2020	Introduction	Cramming More Components Onto Integrated Circuits, G.E. Moore, Proceedings of the IEEE 86(1):82-85, Jan 1998			
10/07/2020	Performance Evaluation (I)	Chapter 1			Reading Quiz
10/12/2020	Performance Evaluation (II)	Andrew Davison, "Twelve Ways to Fool the Masses When Giving Performance Results [illegible]" M. D. Hill and M. R. Marty, "Amdahl's Law in the Multicore Era," in Computer, vol. 41, no. [illegible] V. Sze, Y. -H. Chen, T. -J. Yang and J. S. Emer. How to Evaluate Deep Neural Network Processors: TOPS/W (alone) Considered Harmful. in IEEE Solid-State Circuits Magazine, vol. 12, no. 3, pp. 28-41, Summer 2020.			Reading Quiz
10/14/2020	Memory Hierachy	Appendix B.1-B.4			Reading Quiz
10/19/2020	Memory Hierachy (II)	Chapter 2.1-2.3			Homework #1
10/21/2020	Memory Hierachy (III)	Norman P. Jouppi. 1990. Improving direct-mapped cache performance by the addition of a small full [illegible] SIGARCH Comput. Archit. News 18, 2SI (June 1990), 364–373.			Reading Quiz
10/26/2020					Homework #2
10/28/2020	Virtual Memory	Basu, Arkaprava, et al. "Efficient virtual memory for big memory servers." ACM SIGARCH Computer Architecture News 41.3 (2013): 237-248. Barr, Thomas W., Alan L. Cox, and Scott Rixner. "Translation caching: skip, don't walk (the page table)." *ACM SIGARCH Computer Architecture News* 38.3 (2010): 48-59.			Reading Quiz
11/02/2020	Basic Processor Design	Appendix C.1, Appendix C.2, Chapter 3.1			Reading Quiz
11/04/2020	Branch prediction	Chapter 3.3 M. Evers, S. J. Patel, R. S. Chappell and Y. N. Patt, "An analysis of correlation and predictability: what makes two-level branch predictors work," Proceedings. 25th Annual International Symposium on Computer Architecture (Cat. No.98CB36235), Barcelona, Spain, 1998, pp. 52-61. Retrospective: a study of branch prediction strategies, James E. Smith, ISCA '98: 25 years of the international symposia on Computer architecture (selected papers), New York, NY, USA, 1998, pages 22-23			Reading Quiz
11/09/2020	Branch Prediction	Jiménez, Daniel A., and Calvin Lin. "Dynamic branch prediction with perceptrons." Proceedings [illegible] Seventh International Symposium on High-Performance Computer Architecture. IEEE, 2001. André Seznec. The L-TAGE branch predictor. Journal of Instruction Level Parallelism (http://www.jilp.org/vol9/v9paper6.pdf)			Homework #3
11/11/2020	Veterans Day	**Midterm due 11/13/2020**			
11/16/2020	OOO Scheduling	Chapter 3.4			Reading Quiz
11/18/2020	OOO Scheduling	K. C. Yeager, "The Mips R10000 superscalar microprocessor," in IEEE Micro, vol. 16, no. 2, pp. 28-41, April 1996. R. E. Kessler, "The Alpha 21264 microprocessor," in IEEE Micro, vol. 19, no. 2, pp. 24-36, March-April 1999.			
11/23/2020	OOO Scheduling				Reading Quiz, Homework #4
11/25/2020	SMT	Chapter 3.11 Exploiting choice: instruction fetch and issue on an implementable simultaneous multithreading processor, Dean M. Tullsen, Susan J. Eggers, Joel S. Emer, Henry M. Levy, Jack L. Lo, and Rebecca L. Stamm, ISCA '96: Proceedings of the 23rd annual international symposium on Computer architecture, New York, NY, USA, 1996, pages 191-202. Y. Solihin, Jaejin Lee and J. Torrellas, "Using a user-level memory thread for correlation prefetching," Proceedings 29th Annual International Symposium on Computer Architecture, Anchorage, AK, USA, 2002, pp. 171-182.			
11/30/2020	CMP	The case for a single-chip multiprocessor, Kunle Olukotun, Basem A. Nayfeh, Lance Hammond, Ken Wilson, and Kunyung Chang, SIGPLAN Not. 31(9):2-11, 1996.			Reading Quiz
12/02/2020	Modern Processors	D. Suggs, M. Subramony and D. Bouvier, "The AMD "Zen 2" Processor," in IEEE Micro, vol. 40, no. [illegible] 0.2974217. P. Hammarlund et al., "Haswell: The Fourth-Generation Intel Core Processor," in IEEE Micro, vol. [illegible]			Reading Quiz
12/07/2020	Dark Silicon	H. Esmaeilzadeh, E. Blem, R. S. Amant, K. Sankaralingam and D. Burger, "Dark silicon and the end of multicore scaling," 2011 38th Annual International Symposium on Computer Architecture (ISCA), San Jose, CA, 2011, pp. 365-376. Single-ISA Heterogeneous Multi-Core Architectures: The Potential for Processor Power Reduction, Rakesh Kumar, Keith Farkas, Norm P. Jouppi, Partha Ranganathan, Dean M. Tullsen, In 36th International Symposium on Microarchitecture, December, 2003.			Project
12/09/2020	TPU, FPGA	In-Datacenter Performance Analysis of a Tensor Processing Unit J. Fowers et al., "A Configurable Cloud-Scale DNN Processor for Real-Time AI," 2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture (ISCA), Los Angeles, CA, 2018, pp. 1-14.			Homework #5
12/15/2020	Final Exam	**Due 12/15/2020 By 11am**			

Performance

Memory

Processor

Parallelism

Subject to change

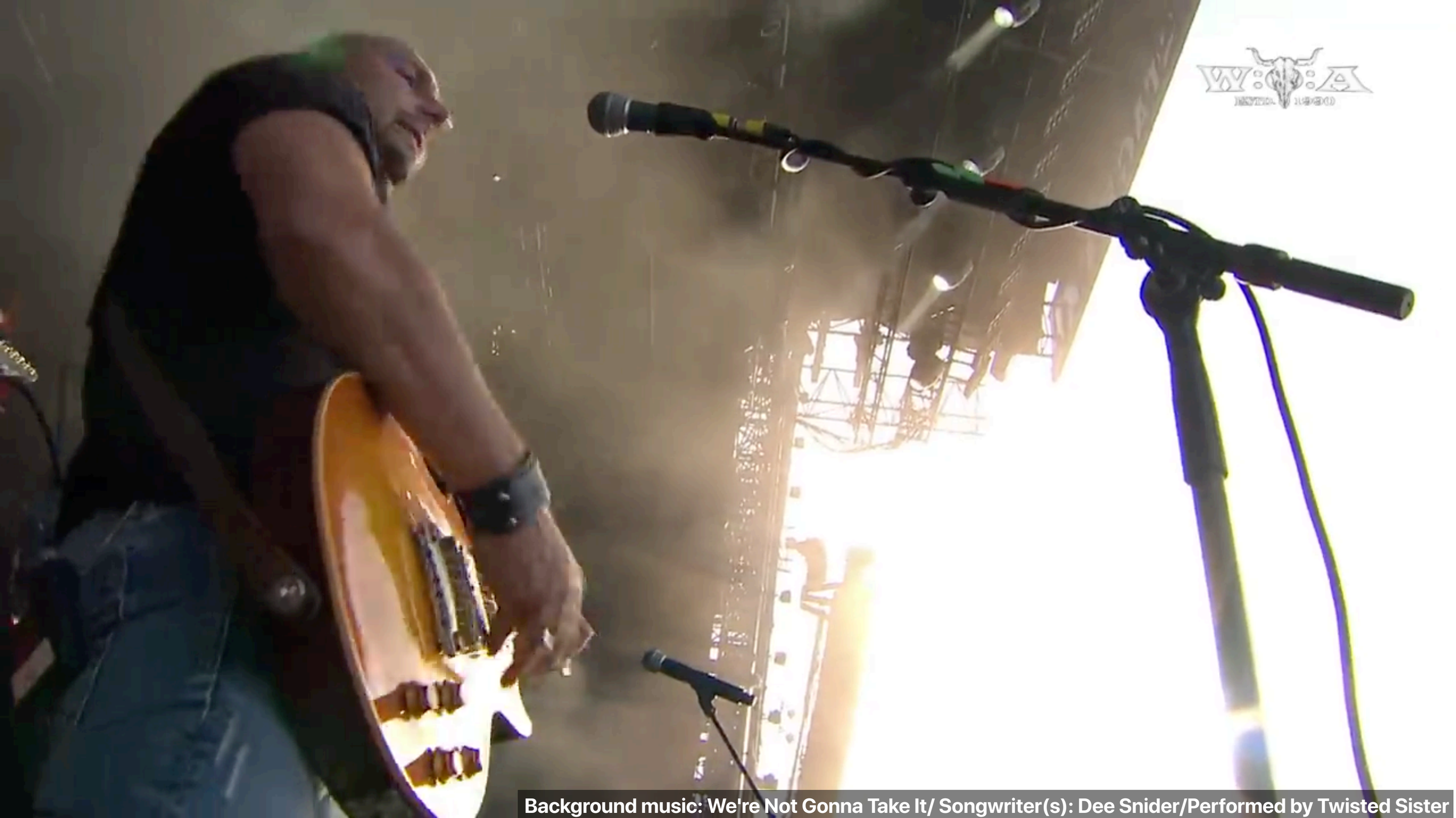
You need to complete the reading of H&P and papers

Download Slides/ Check due dates here

Learning eXperience

Your tasks

- Login/discussion in **eLearn** and **piazza**.
- Read the text before class!
  - **Computer Architecture: A Quantitative Approach (6th Edition)**
    by John Hennessy and David Patterson — previous editions are not supported
  - **I'm not going to cover everything in class, but you are responsible for all the assigned text**.
  - Papers
- Reading quizzes in **eLearn** (15%) — will drop the lowest two
- Homework throughout the course. (15%) — will drop the lowest one
- Class participation (5%)
- Project (10%)
- Midterm (20%)
- Cumulative final (35%)


Background music: We're Not Gonna Take It/ Songwriter(s): Dee Snider/Performed by Twisted Sister

Most lectures today …


Me
I expect the lecture to be...
You

Peer instruction

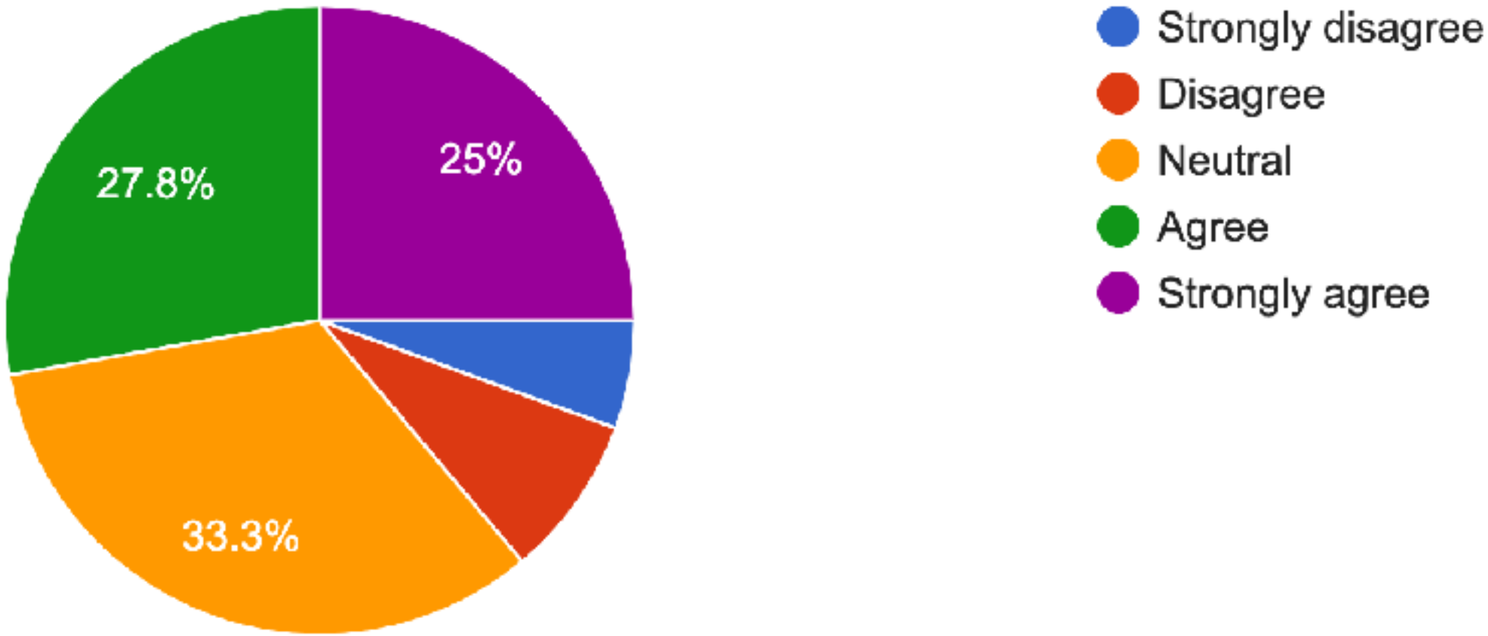
- Before the lecture — You need to complete the required **reading**
- During the lecture — I'll bring in activities to ENGAGE you in exploring your understanding of the material
  - Popup questions
  - Individual **thinking** — use your clicker to express your opinion
  - Group **discussion** — discuss with your surroundings and use your clicker to express your group's opinion
  - Whole-classroom **discussion** — we would like to hear from you

Read **Think** **Discuss**

Try your best to discuss

Under the indoor mask mandate, I feel comfortable to discuss with a few people sitting nearby my seat.

36 responses



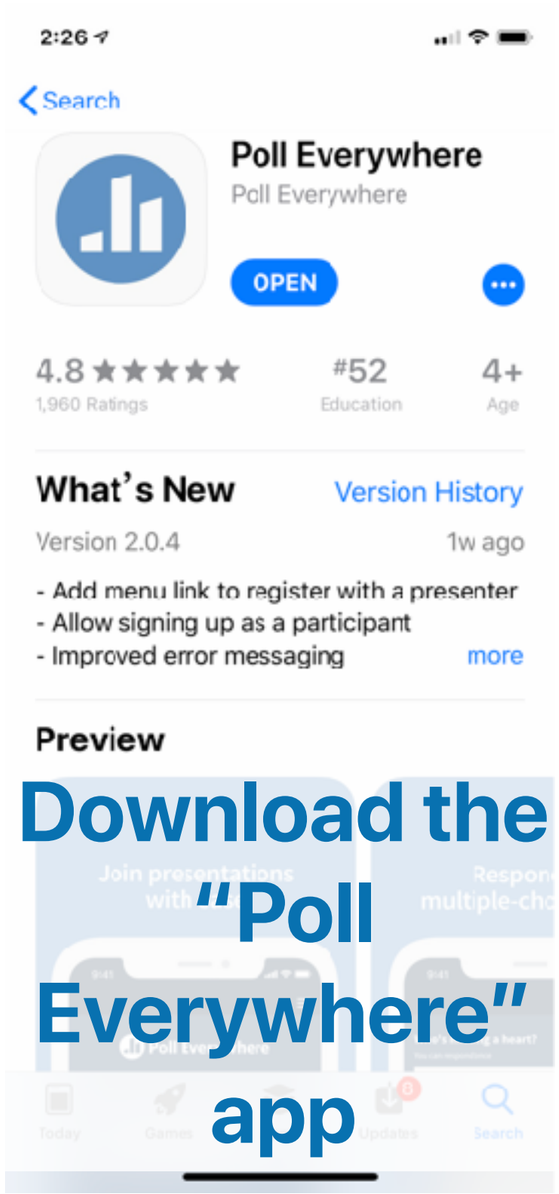
Why reading quizzes?

- We need to **prepare** you for peer instruction activities and discussions!
- Reading assignments from
  - **Computer Architecture: A Quantitative Approach (6th Edition)**
    by John Hennessy and David Patterson
  - Papers
- Reading quizzes:
  - On eLearn
  - Due **before** the lecture, usually once a week. Check the schedule on our webpage
  - You will have **two** chances. We take the **average**
  - No time limitation until the deadline
  - **No make up** reading quizzes — we will **drop** probably **two lowest** at least

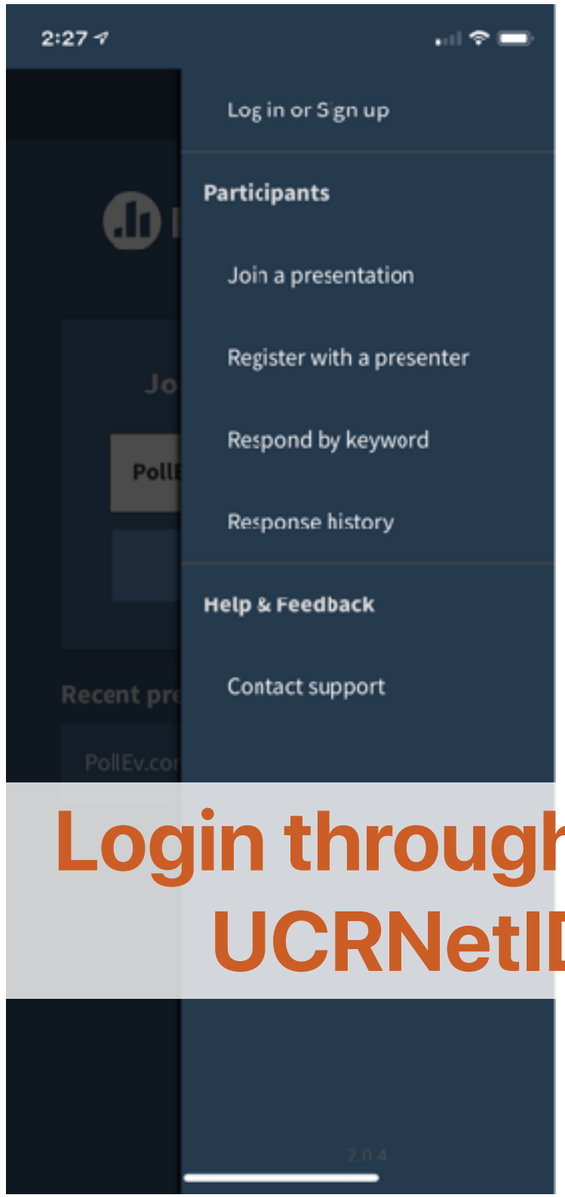
Peer instruction

- I'll bring in activities to ENGAGE you in exploring your understanding of the material
  - Let you practice
  - Bring out misconceptions
  - Let us LEARN from each other about difficult parts.
- You will be GET CREDIT for your efforts to learn in class
  - By answering questions with **Poll Everywhere**
  - Answer **50%** of the **clicker questions** in class, get 5% of your final grade
    - Typically more than 50% of questions are individual thinking questions as individual thinking comes first
    - If you don't feel comfortable to talk with others, you can still get full credits if you made choices on all individual thinking questions

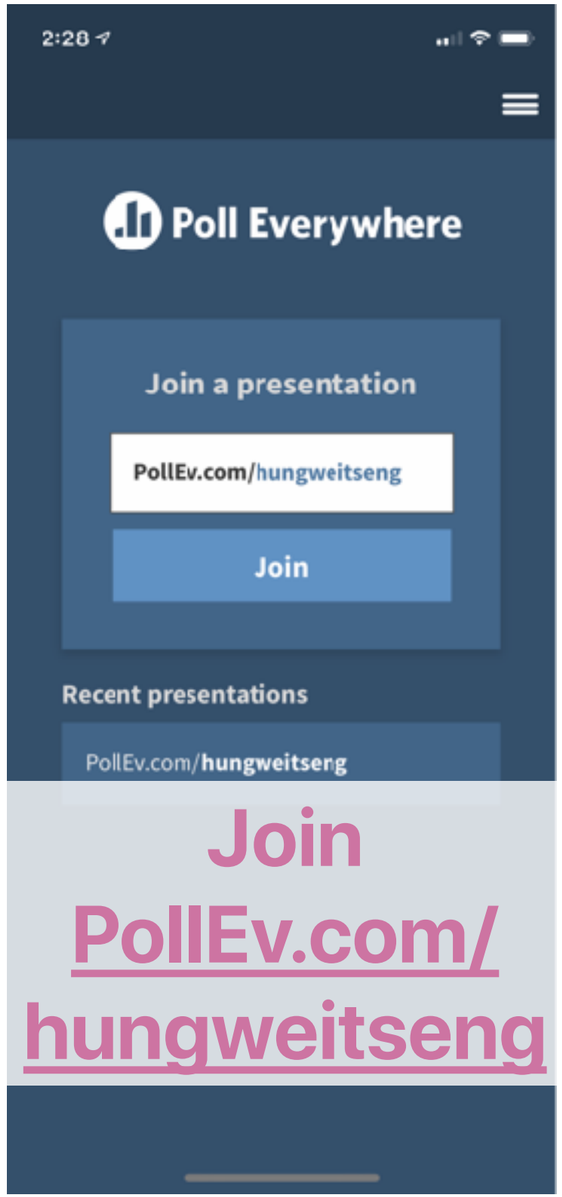
About the time of the Lecture — Setup Poll Everywhere



Download the "Poll Everywhere" app



Login through the app using UCRNetID@ucr.edu



Join PollEv.com/hungweitseng

Why still assignments and term project?

- Human beings' memories are volatile and vague
- Assignments
  - Let you practice again the concepts learned from the lectures
  - The best way to prepare for midterm and final
  - Publish on the website, submit through iLearn
- Project
  - Let you get a feeling how you can apply the knowledge learned in class to "real-life" applications/program
  - C/C++ programming
  - Individual project
  - It's going to be a "contest" — the winner will have a prize

Logistics

Course resource

- Lectures:
  - MW 9:30a—10:50a @ Olmsted 1208
- Living streaming, video recording
  https://www.youtube.com/profusagi
- Schedule, slides on **course webpage**:
  https://www.escalab.org/classes/cs203-2021fa/
- Discussion on **piazza**:
  https://piazza.com/class/ktq8dff9z053pw
- Reading quizzes, homework submissions on **eLearn**:
  https://elearn.ucr.edu

The website

- Calendar
- Schedule
- Slides
  - Preview — for the ease of note taking
  - Release — the actual slides

CS203: Advanced Computer Architecture (2021 Fall

Lecture: **MW 9:30a – 10:50a**

Where: **UCR Campus Olmsted 1208**

Schedule and Slides | Assignments and Project

Instructor

Hung-Wei Tseng
email: htseng @ ucr.edu
Office Hours: TBA

Teaching Assistant

TBA

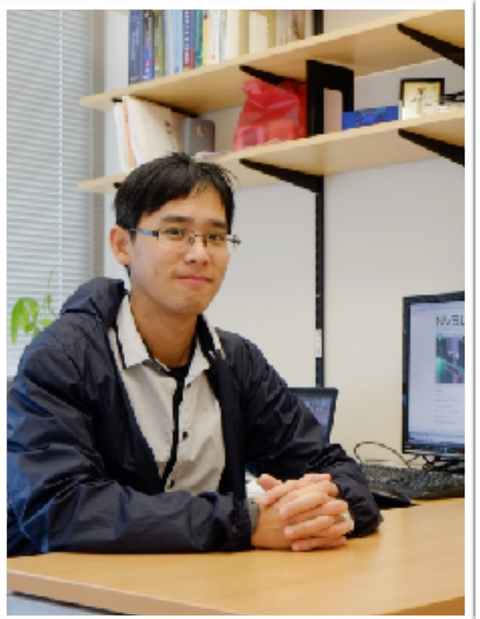
Other important links

Quizzes, Assignments, Grading: eLearn
Discussion Forum on Piazza: https://piazza.com/class/ktq8dff9z053cw
Youtube Channel/Video Archive: https://www.youtube.com/profusapi

Hung-Wei's Lectures/Office Hours

Instructor — Prof. Usagi (a.k.a. Hung-Wei Tseng)

- Website: https://intra.engr.ucr.edu/~htseng/
- E-mail: htseng @ ucr.edu
- PhD in **Computer Science**, University of California, San Diego
- Research Interests
  - General-purpose computing on AI/ML/NN accelerators
  - Intelligent storage devices & near-data processing
  - Or anything else fun — we have an OpenUVR project recently
- Office hour: MTu 2p-3p @ WCH 406 or through Zoom (will share the link on eLearn)



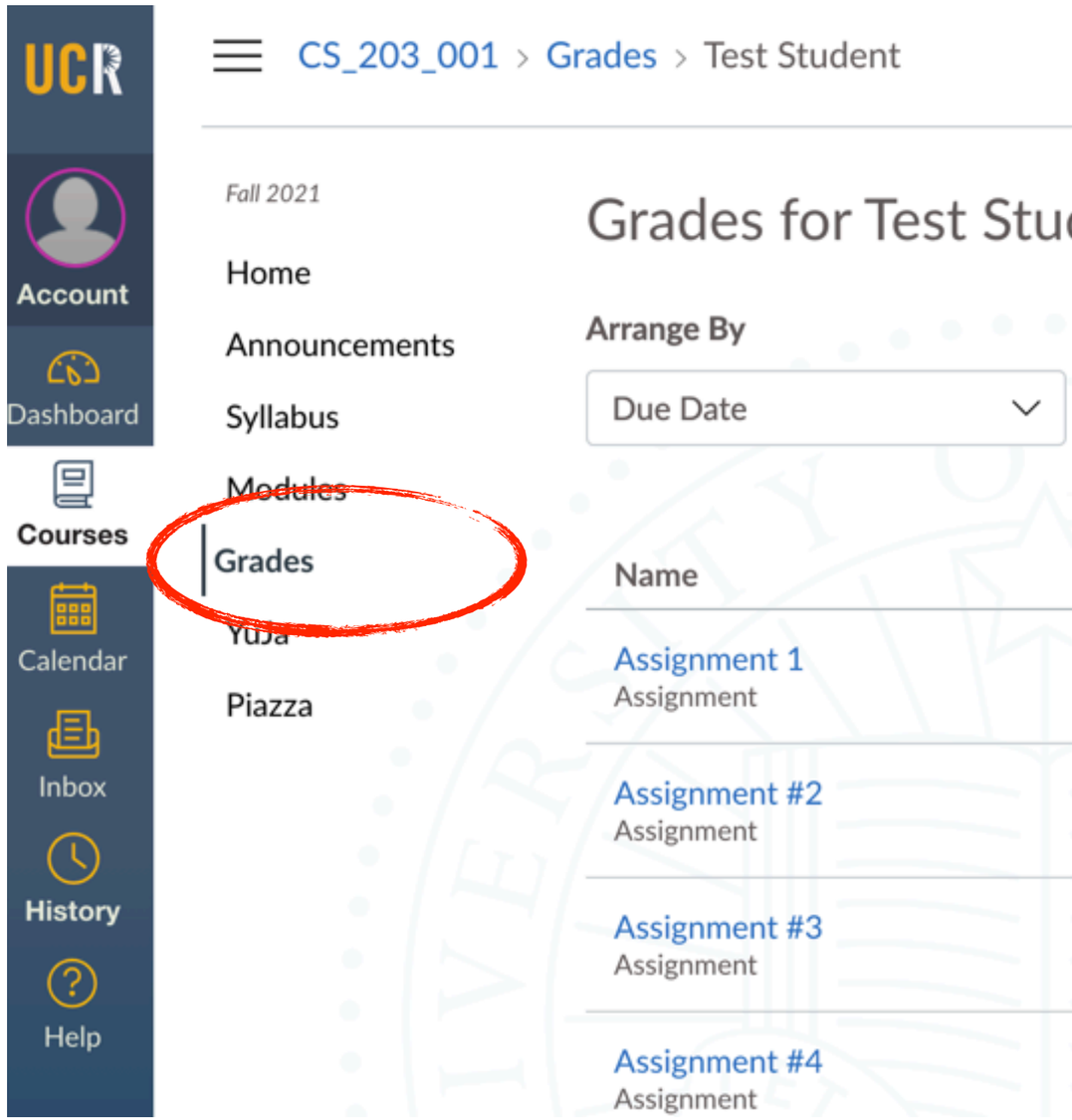
Teaching Assistant — Abenezer Wudenhe

- Office hours: WTh 3p-4p on Zoom

- E-mail: awude001 @ ucr.edu

Grading

- You can see your grades on eLearn.
- Errors in grading
  - If you feel there has been an error in how an assignment or test was graded, you have **one week** from when the assignment is return to bring it to our attention.
  - You **MUST** submit (via email to the instructor AND the appropriate TAs) a written description of the problem. Neither I nor the TAs will discuss regrades without receiving an email from you about it first.
- For arithmetic errors (adding up points etc.)
  - you do not need to submit anything in writing, but the **one-week** limit still applies.



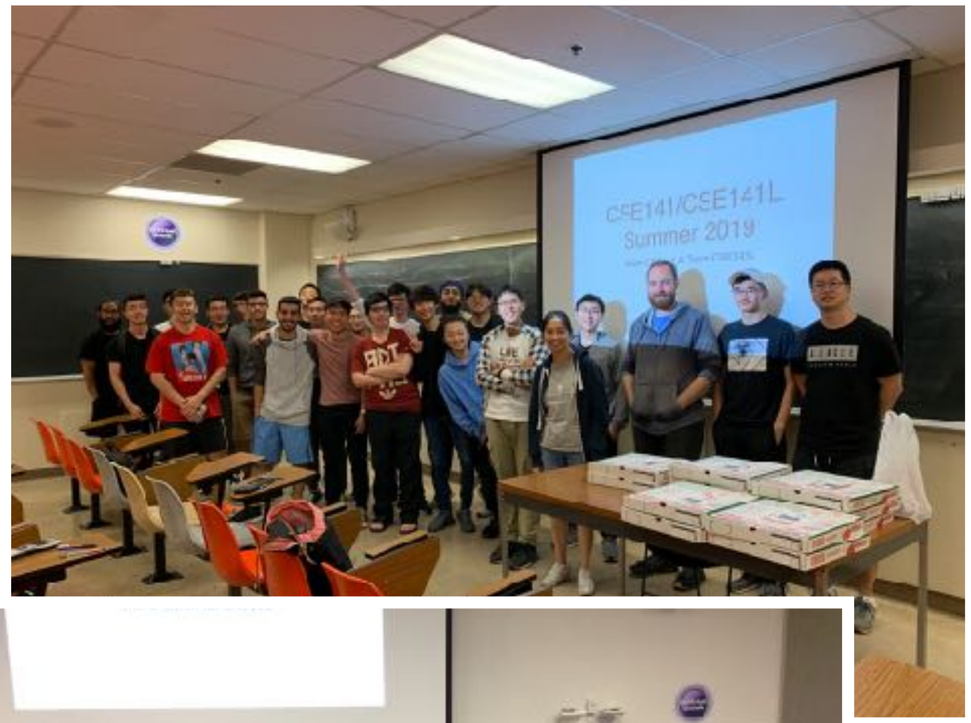
Academic Honesty

- Don’t cheat.
  - Cheating on a test will get you an F in the class and no option to drop, and a visit with your college dean.
  - Cheating on homework means you don’t have to turn them in any more, but you don’t get points either. You will also take at least 25% penalty on the exam grades.
- Copying solutions of the internet or a solutions manual is cheating
  - They are incorrect sometimes
- Review the UCR student handbook
- When in doubt, ask.

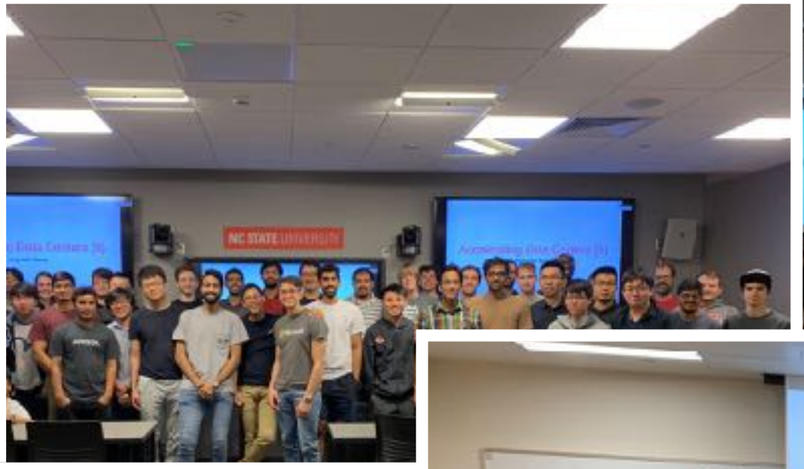
Term of Service

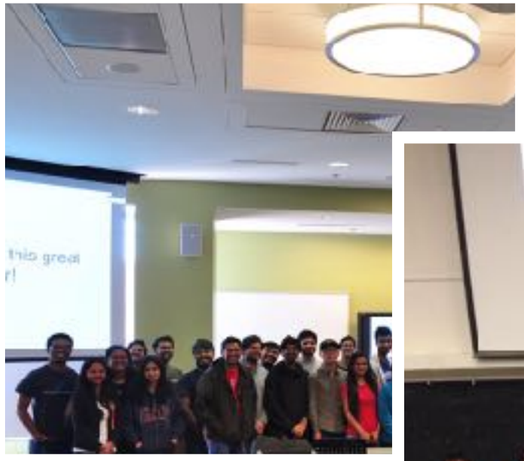
- CS203 is an **Advanced Computer Architecture** class for graduate students. It's not our responsibility to recap everything that should be covered by an undergraduate computer architecture class from a regular computer science undergraduate program.
- This class requires **intensive readings** in research papers and the assigned textbook.
- This class requires you to **speak and discuss** your opinion with your classmates as well as the instructor.
- This class requires **programming projects** that uses the **C programming language**. It is **your responsibility to learn how to program in C**. It is also your responsibility to design the architecture, implementation details and tests for your coding projects.
- The instructor and course staffs reserve the right to refuse to answer inappropriate questions (e.g. directly telling if an answer is right or not).
- **It is your responsibility to track the latest schedule, information, grades and materials from our course website, e-mails from the course staffs and the piazza forum.**
- Any cheating will be treated seriously. You will get an F and we will report to the Dean's office

By clicking this box, you are agreeing to the Terms and Conditions of CS 203, Fall 2021.



CSE141/CSE141L
Summer 2019









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Before you leave the classroom…

- Login piazza, eLearn
- Check our website — where you can find our slides (including this one), the schedule, the syllabus, the complete schedule of classes
- Reading quiz due this Wednesday **before** the lecture
- Get ready for Poll Everywhere
  - Download the Poll Everywhere App to your phone
    or
  - Bring a laptop that can browse https://pollev.com/hungweitseng
    and
  - Login with UCRNetID@ucr.edu — that's the most important. If you didn't do it right, you won't get credits.

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