Due: April 7th 11:59 pm PCT

LABORATORY # 1

Xilinx Environment

Lab1 is a preparation for future labs. In lab1, you will:

Install the Xilinx ISE for the Verilog Project.

Build a basic project with schematic design.

Write a testbench to test your design.

Analysis the simulation result.

Install the Xilinx ISE

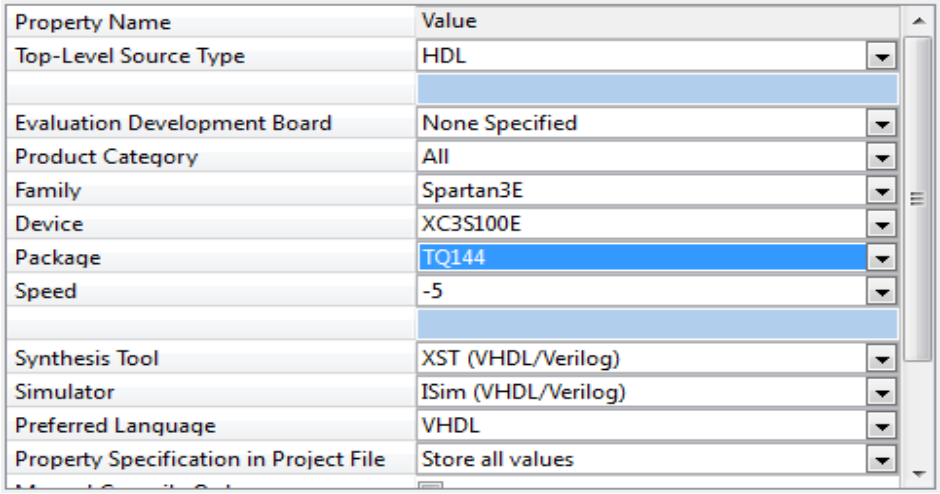
There are a few items you should address to be fully prepared for lab. Please complete all items before your first lab as this process can take a few hours:

1. Please create an account for downloading Xilinx:
https://www.xilinx.com/registration/create-account.html
2. Please install "Webpack" version, you can get the key from
https://www.xilinx.com/support/licensing_solution_center.html
3. Once you want to use the software, please always try the 32-bit project navigator from start menu instead of clicking the icon on the desktop
4. Watch the video before you start the followings.

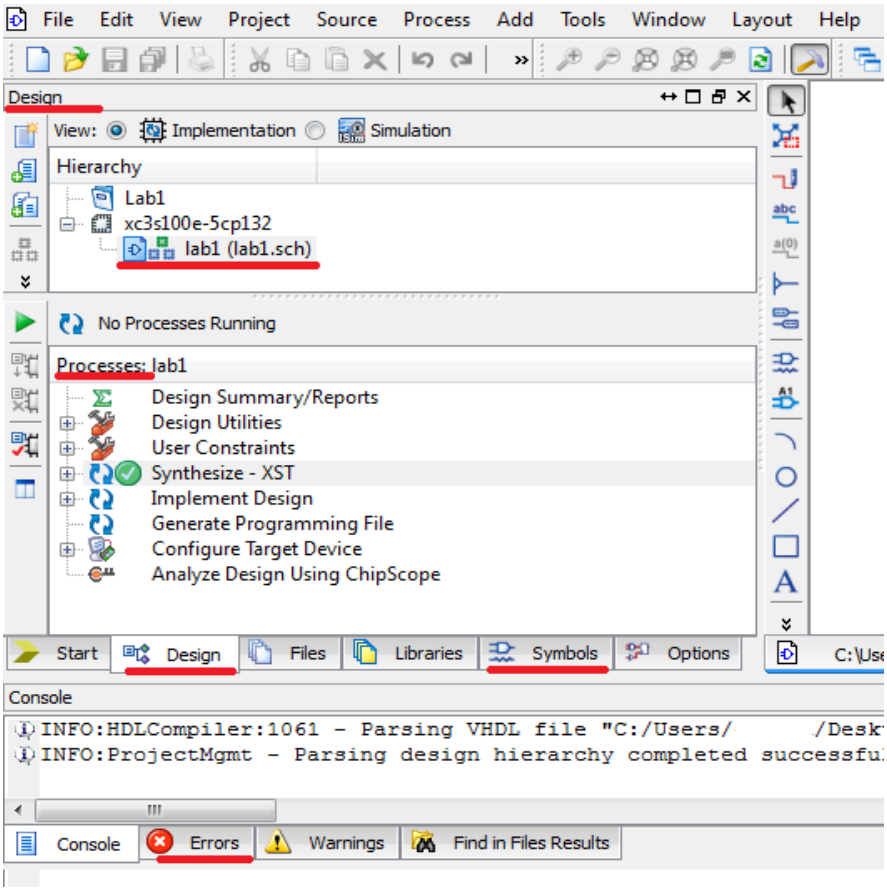
Build a new project with schematic design:

1. Open Xilinx ISE “32-bit Project Navigator” and click File>New Project
2. Enter a “Project name” and select a “Project location” for your project.
3. Select “Schematic” as your “Top-level source type” and click next.

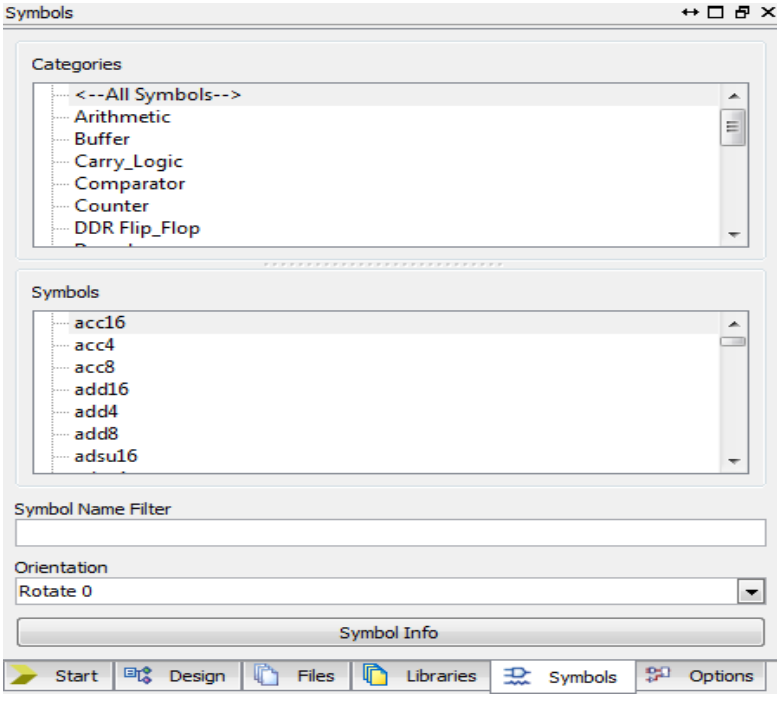
Your next window should look EXACTLY like this EXCEPT for Top-Level Source Type



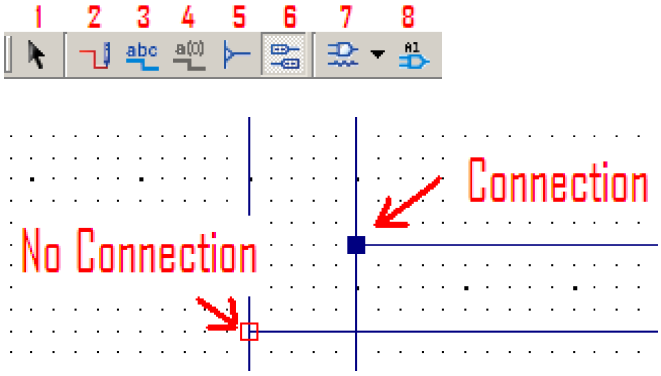
5. Click “New Source,” select “Schematic,” enter a “File name”, you should see something like this:



6. Click the “Symbols” tab. At this point it is a good idea to make the Symbols window longer, so you can see more of the list of symbols available for use.



7. Find And2, Nand2, Or2, Nor2 gate, connect those gates to use common inputs.



8. From the schematic sidebar, select the “Add I/O Marker” icon. Now click each input and output. A marker will now be created with a name XLXN_XX, where XX is a number.

9. At this point, save your schematic. You now need to synthesize your schematic to simulate it.

Write a testbench

10. Back in the Design window, right click and select new source. Choose “Verilog Test Bench,” type in a name. You should see your test bench open.

11. The facilitate this task, the following template is given

```
module test_test_sch_tb();

// Inputs
    reg Bot;    reg Top;

// Output
    wire A;     wire B;     wire C;     wire D;

// Clk
reg clk;

// Instantiate the UUT
    Lab1 UUT (
        .A(A),
        .B(B),
        .C(C),
        .D(D),
        .Bot(Bot),
        .Top(Top) );
```

```
    initial begin
      clk = 0 ;
      forever begin
            #20 clk = ~clk;
      end
    end

      initial begin

      #40 ;
      Bot = 1'b0;
      Top = 1'b0;
      #40 ;
      $display("TC21");
      if ( {A,B,C,D} != 4'b0101 ) $display    ("Result is wrong %b ", {A,B,C,D});

      // Your own test cases start here

     // Your own test cases end here
      end

endmodule
```

12. The template test the situation with (Top, Bot)=00, you will need to finish other possible input situations.

13. Make sure your test bench is selected in the Design window. In the options displayed in the Processes window expand the “ISim Simulator” and double click “Simulate Behavioral Model.” The simulation window will open up.

Please Answer the following Questions in your report!

Question1: In the testbench, explain your understanding of this syntex:

```
// Instantiate the UUT
    Lab1 UUT (
        .A(A),
        .B(B),
        .C(C),
        .D(D),
        .Bot(Bot),
        .Top(Top) );
```

Question2: How many possible input states in the test bench?

Question3: What's the frequency of clock signal in the testbench?

Question4: Please paste your testbench code.

Question 5: Please paste your schematic design screenshot.

Question 6: Please paste your simulation waveform screenshot.