LABORATORY # 3

In lab3, you will:

Study the 7-segment LED display and LED decoder.

Build a basic project with behavior design, which uses switches to control the LED display.

Write a testbench to test your design.

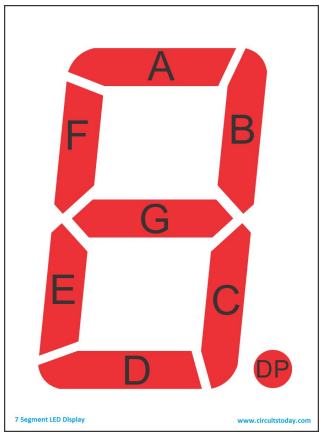
Analysis the simulation result.

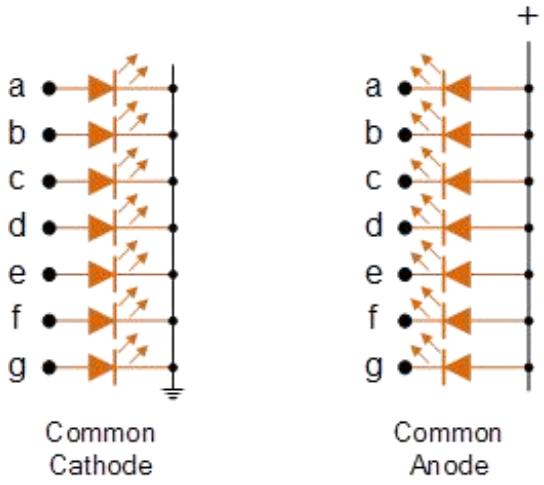
Learn the 7-segment LED display.

1. There are a few items you should know at the beginning. Please read and learn(before the lab) the 7-segment LED display from this link:

https://www.electronics-tutorials.ws/combination/comb_6.html

Briefly speaking, the 7-segments LED display consists of 7 independent LEDs (if you count the DP in, that will be 8 independent LEDs). You can control the LED combination to display numbers through 0-9.





In our lab, the 7-segments LEDs are Common Anode, which means a=0 is light on, a=1 is light off.
If you want to dispaly number “1”, the combination should be abcdefg=7’b1001111, only segment b and segment c are light on.

Build a new project with behavior design:

2. Open Xilinx ISE “32-bit Project Navigator” and click File>New Project

3.. Enter a “Project name” and select a “Project location” for your project.

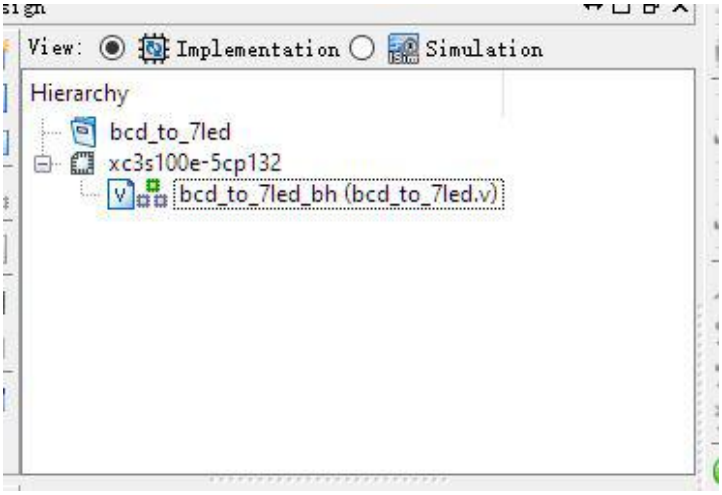
4.. Select “Schematic” as your “Top-level source type” and click next.

Your next window should look EXACTLY like this EXCEPT for Top-Level Source Type

Property Name	Value
Top-Level Source Type	HDL
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3E
Device	XC3S100E
Package	TQ144
Speed	-5
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values

5. Click “New Source,” select “verilog module,” enter a “File name”, delete the .sch file.

   You should see something like this:



Write verilog module

6.**Note, the 7-seg display is active low (0 = on, 1 = off)**

```
module bcd_to_7led_bh (
  input wire sw0 ,      // Switches
  input wire sw1 ,
  input wire sw2 ,
  input wire sw3 ,
  output reg a ,    // LED segments
  output reg b ,
  output reg c ,
  output reg d ,
  output reg e ,
  output reg f ,
  output reg g ,
  output reg an0,    // LED display control (To power on the entire 7-seg display)
  output reg an1,
  output reg an2,
  output reg an3
```

```
   );

// Internal wire
wire [3:0] bundle ;
assign bundle = {sw3,sw2,sw1,sw0 } ;

always @(*) begin

      // Setting the ANs signals (Set AN3 to 0 to turn it on)
      an0 = 1'b1;
      an1 = 1'b1;
      an2 = 1'b1;
      an3 = 1'b0; // Display in the module AN3

      // Setting the segments signals (Initialize all to off/1)
      a = 1'b1 ;
      b = 1'b1 ;
      c = 1'b1 ;
      d = 1'b1 ;
      e = 1'b1 ;
      f = 1'b1 ;
      g = 1'b1 ;

  case ( bundle )

      4'b0000 : begin // 0
            a = 1'b0 ;
            b = 1'b0 ;
            c = 1'b0 ;
            d = 1'b0 ;
            e = 1'b0 ;
            f = 1'b0 ;
                              g = 1'b1 ;        //(Don't need to explicitly state that g is off
here since
                                                //    it is initialized to off already,
but it doesn't hurt)
      end
// Your code goes here
      endcase
end

endmodule
```

7.Do the synthesis.

Write a testbench

8. Back in the Design window, switch to the simulation mode, right click and select new source. Choose "Verilog module" type in a name. You should see your test bench open.
9. The facilitate this task, the following template is given

```
`timescale 1ns / 1ps


module bcdtoled_tb;

    // Inputs
    reg sw0;
    reg sw1;
    reg sw2;
    reg sw3;

    // Outputs
    wire a;
    wire b;
    wire c;
    wire d;
    wire e;
    wire f;
    wire g;

    // Instantiate the Unit Under Test (UUT)
    bcd_to_7led_bh uut (
    // bcdto7led_bh uut (
        .sw0(sw0),
        .sw1(sw1),
        .sw2(sw2),
        .sw3(sw3),
        .a(a),
        .b(b),
        .c(c),
        .d(d),
        .e(e),
        .f(f),
        .g(g)
    );

    initial begin

        // Initialize Inputs
        sw3 = 0;    sw2 = 0;    sw1 = 0;        sw0 = 0;
```

```
        #100;
       $display("TC10 ");
        if ( {a,b,c,d,e,f,g} != 7'b111_1110 ) $display    ("Result is wrong %b ",
{a,b,c,d,e,f,g});


        ##########your code here
        #######


    end

endmodule
```

10.The template test the situation with (sw3,sw2,sw1,sw0)=4'b0000, you will need to finish other possible input situations(decimal value=1,2,3,4,5,6,7,8,9).

11.Make sure your test bench is selected in the Design window. In the options displayed in the Processes window expand the "ISim Simulator" and double click "Simulate Behavioral Model." The simulation window will open up.

Hand in:

Question1: Please write the truth table between Decimal input to LED segments output.

Question2: How many possible input states in the test bench?

Question3: If our 7-segments LED are common Cathode, what will be different in our lab?

Question4: Please paste your verilog code and testbench code.

Question 5: Please paste your simulation waveform screenshot.