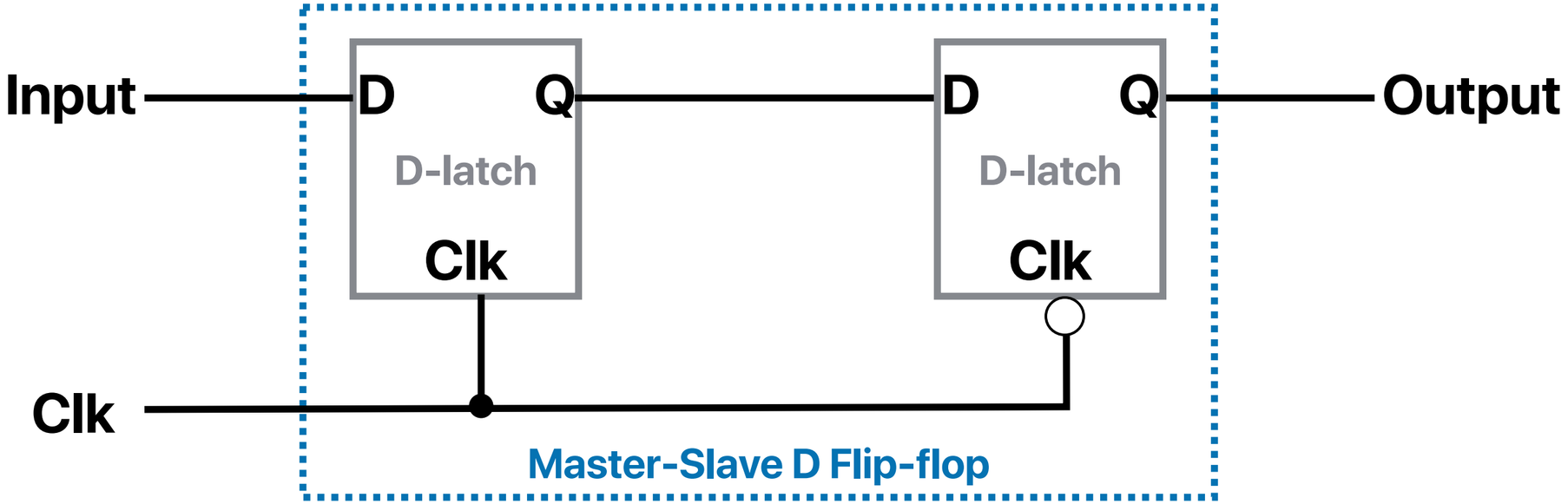
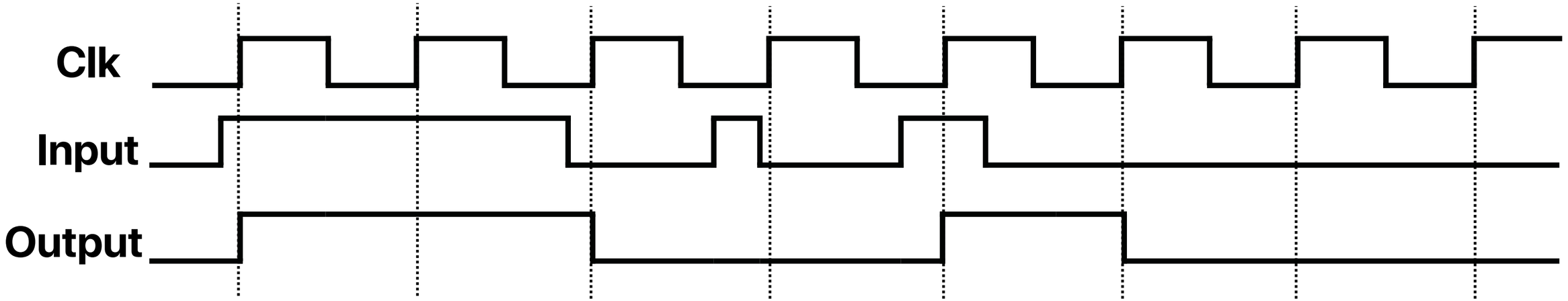
Datapath Components (4) — Those Who Can “Remember” Things

Prof. Usagi

Recap: D flip-flop





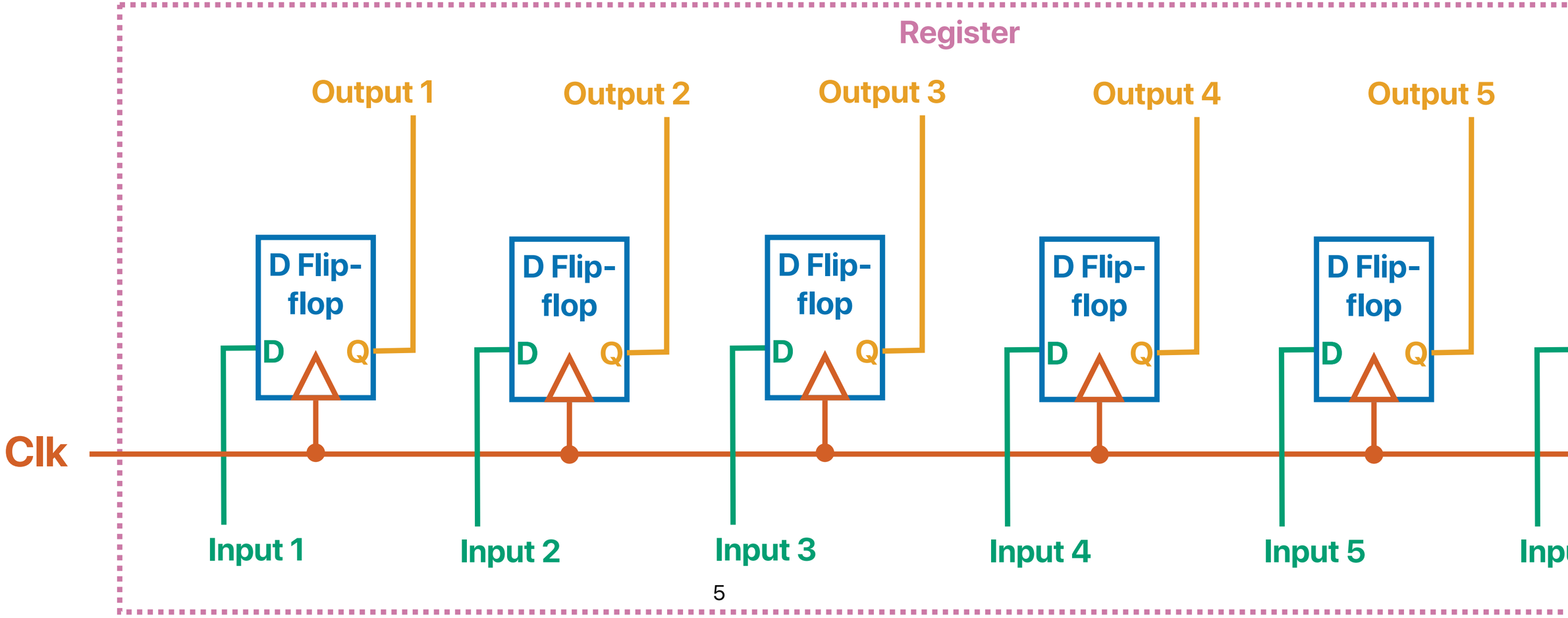
Outline

- Volatile Memory
  - Registers
  - SRAM
  - DRAM
- Non-volatile Memory

Registers

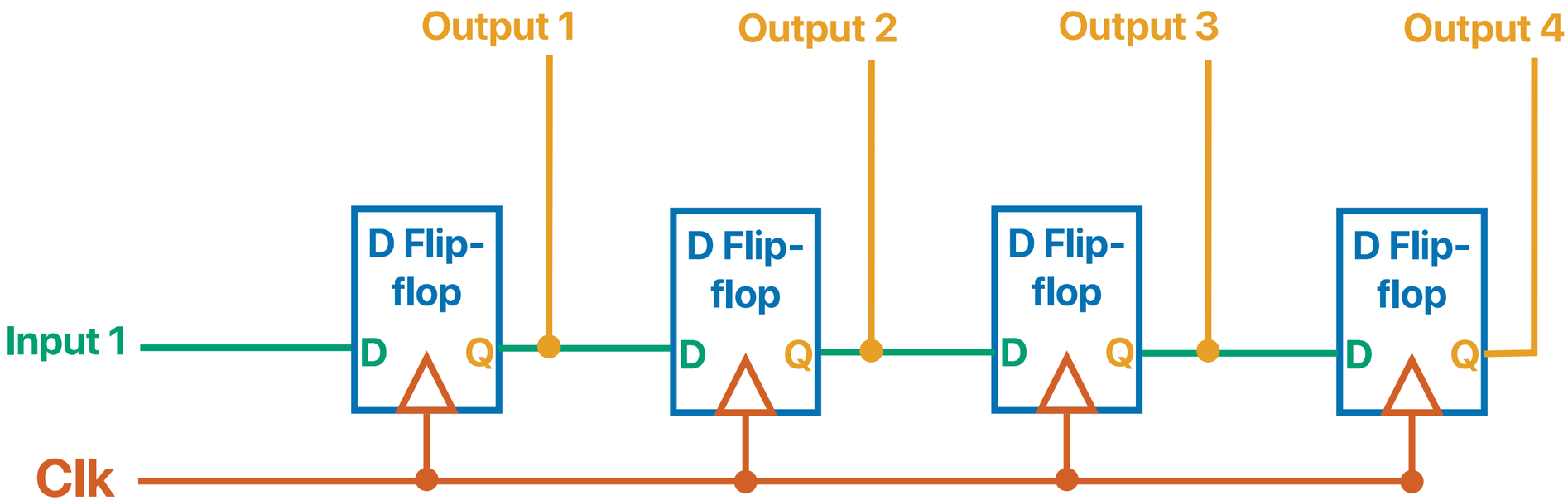
Registers

- Register: a sequential component that can store multiple bits
- A basic register can be built simply by using multiple D-FFs



Shift register

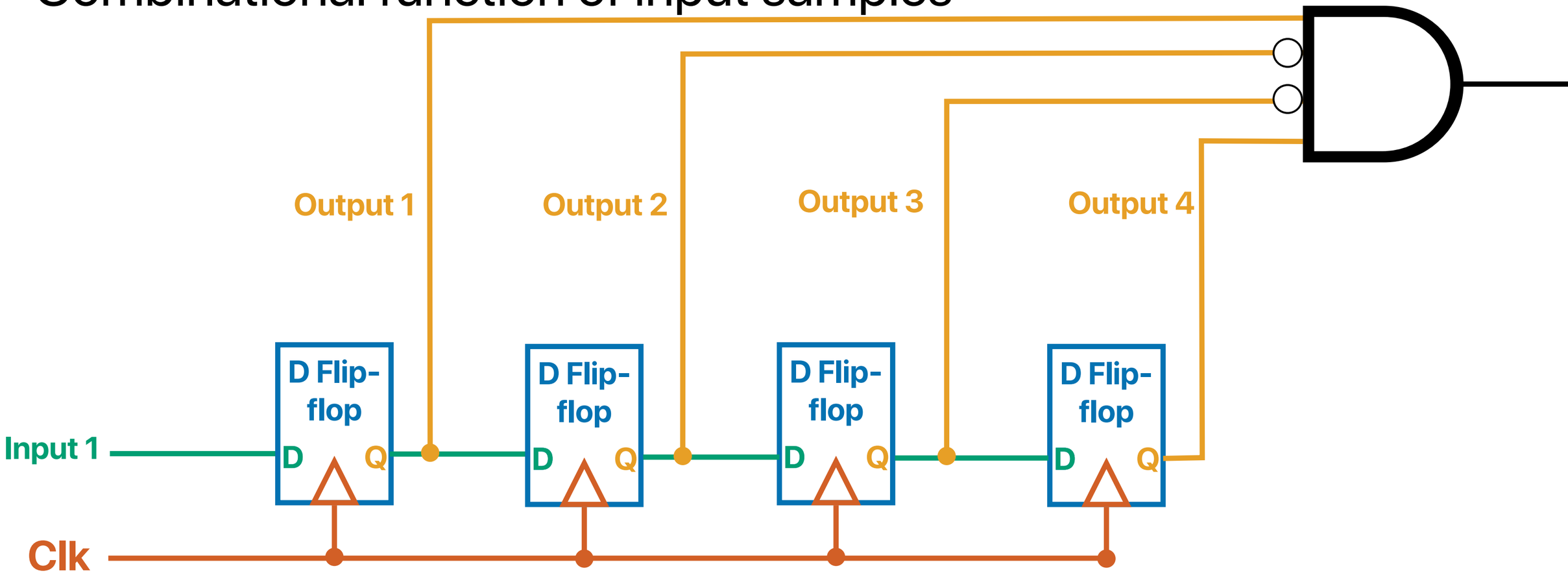
- •Holds & shifts samples of input



Pattern Recognizer

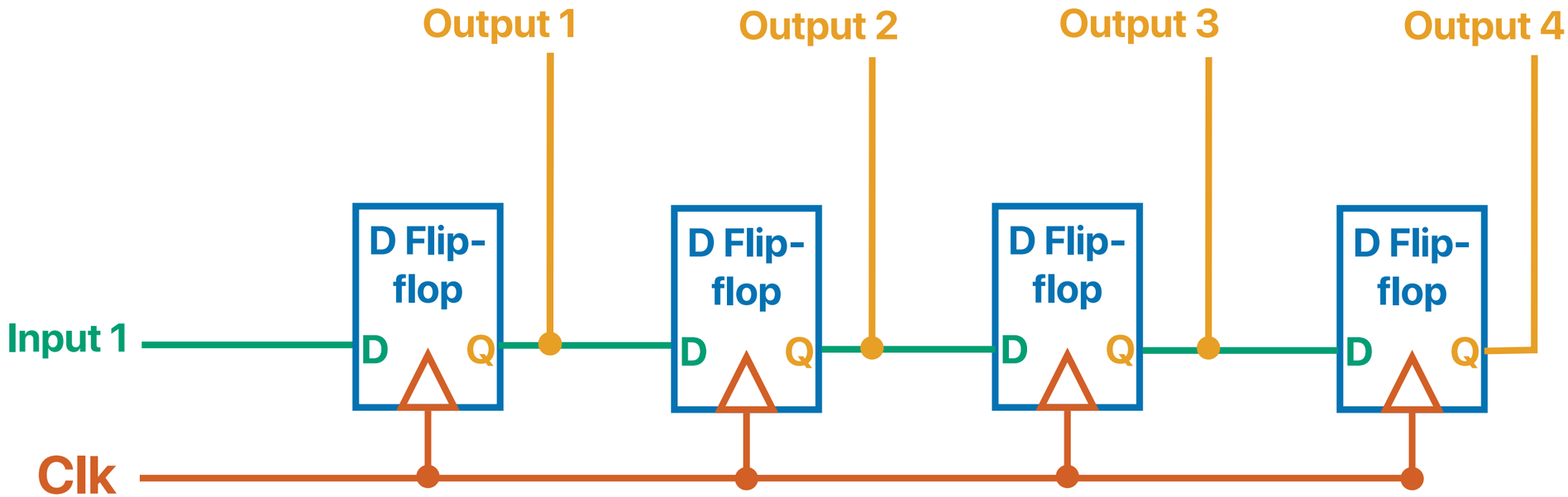
- Combinational function of input samples

We can recognize 1001!



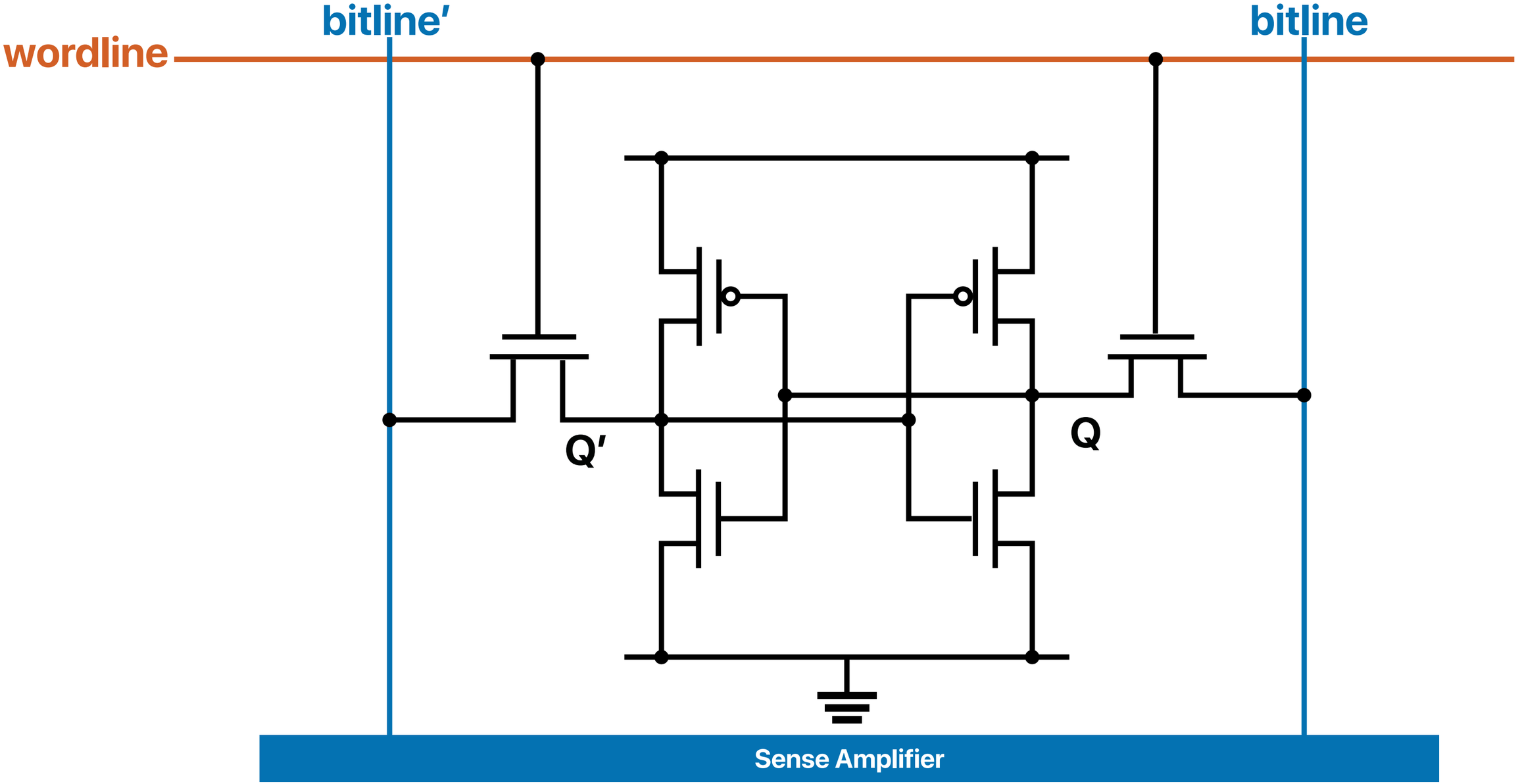
Counters

- Sequences through a fixed set of patterns
- Note: definition is general
- For example, the one in the figure is a type of counter called Linear Feedback Shift Register (LFSR)

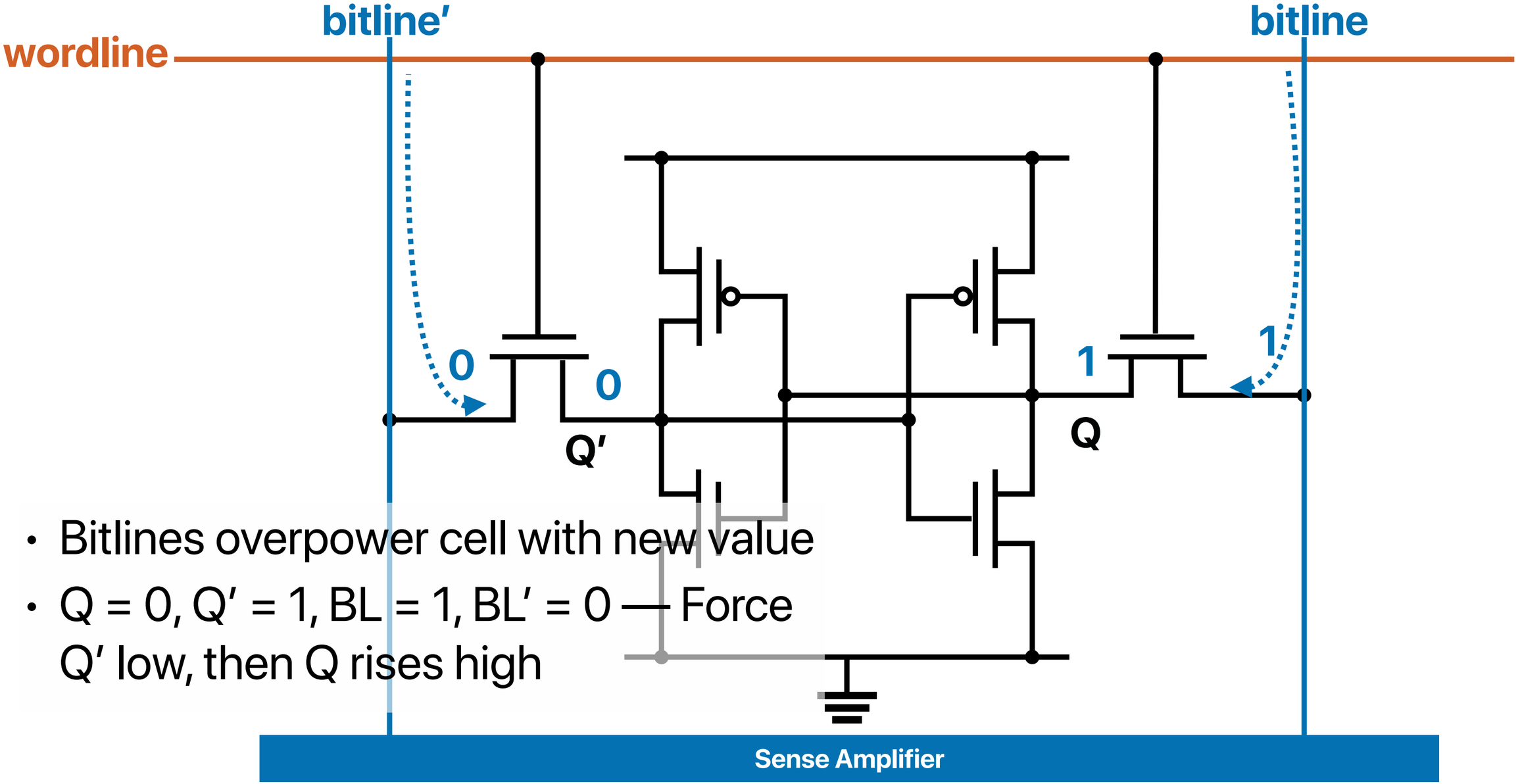


Static Random Access Memory (SRAM)

A Classical 6-T SRAM Cell

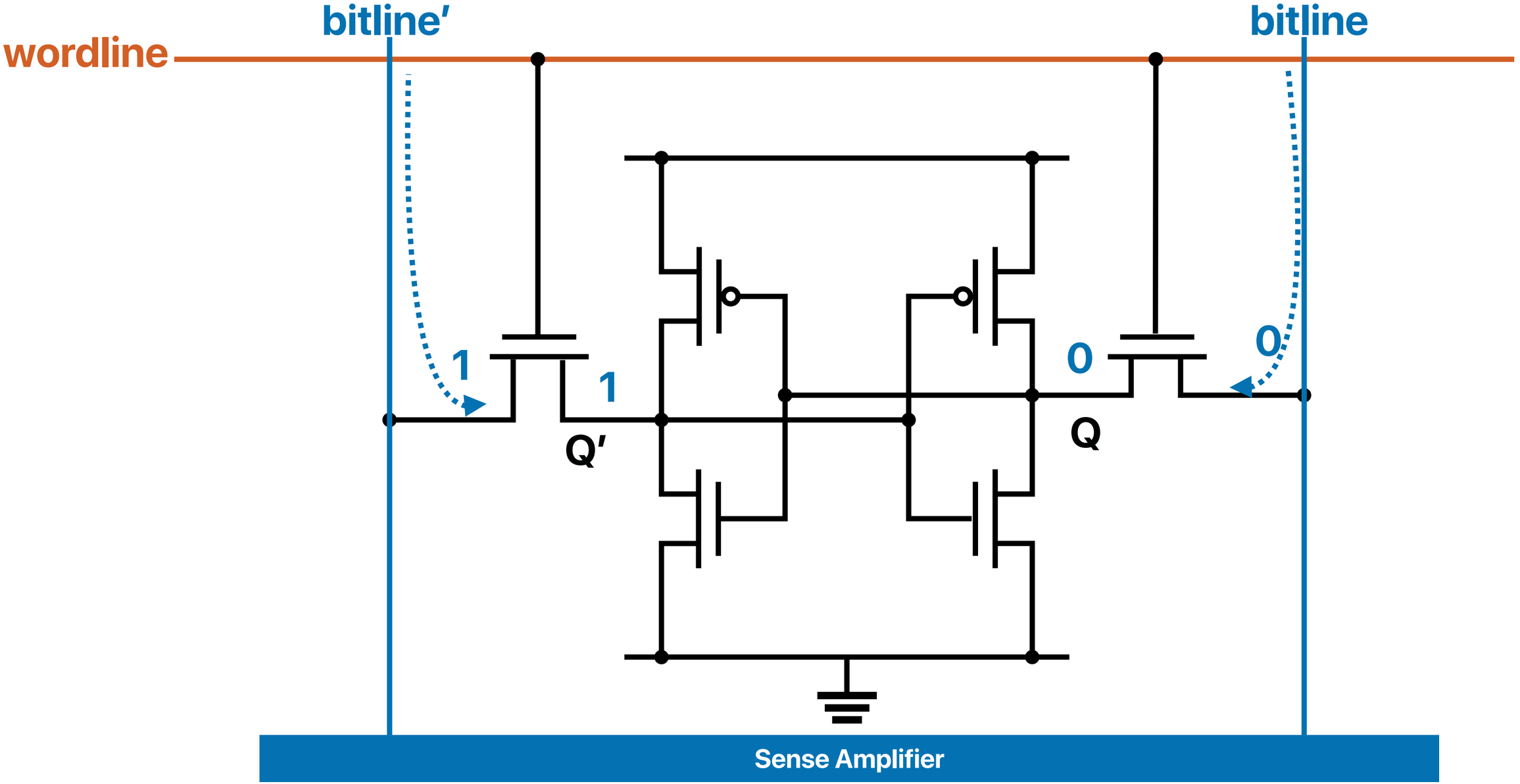


Write “1” to an SRAM Cell

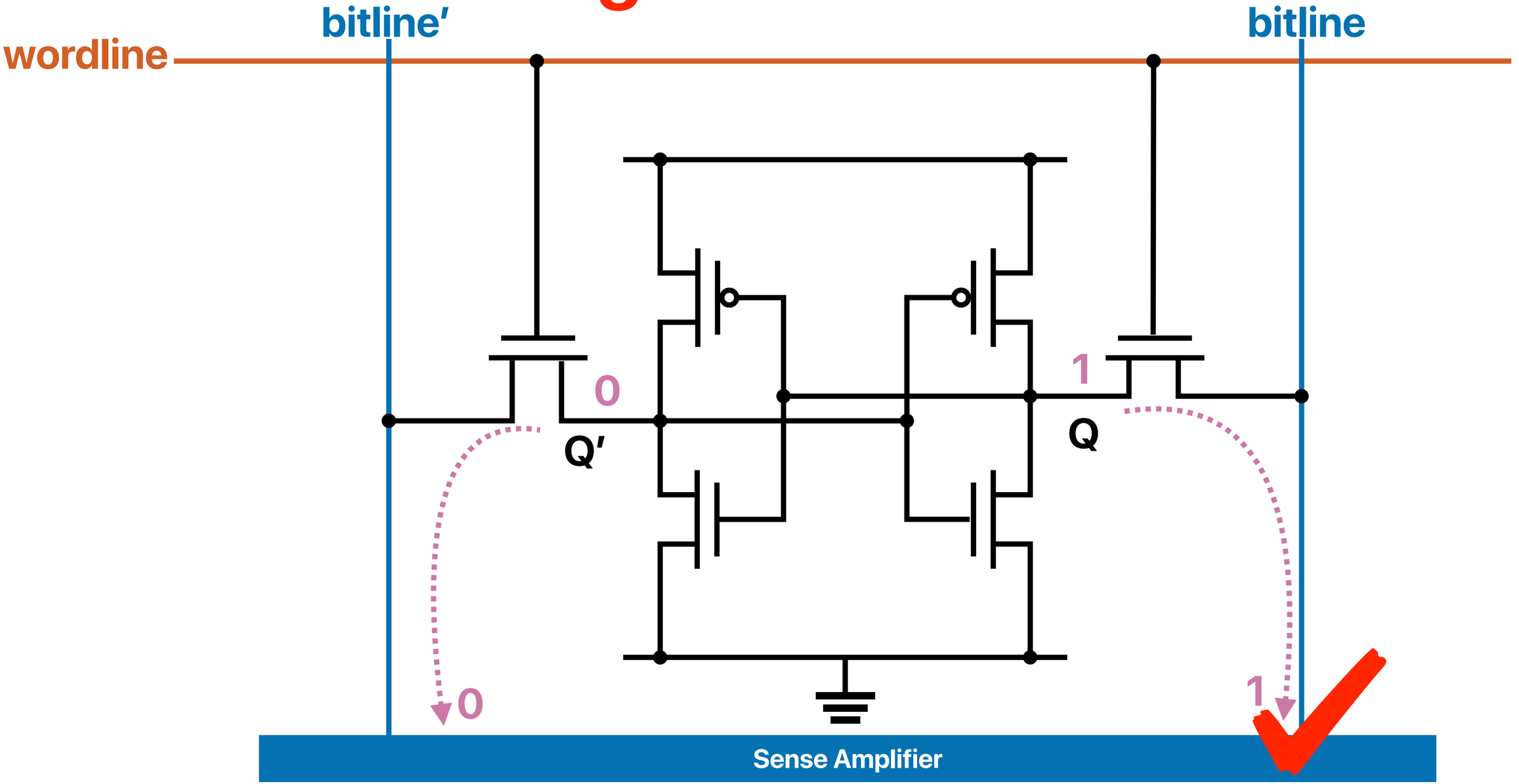


- Bitlines overpower cell with new value
- Q = 0, Q’ = 1, BL = 1, BL’ = 0 — Force Q’ low, then Q rises high

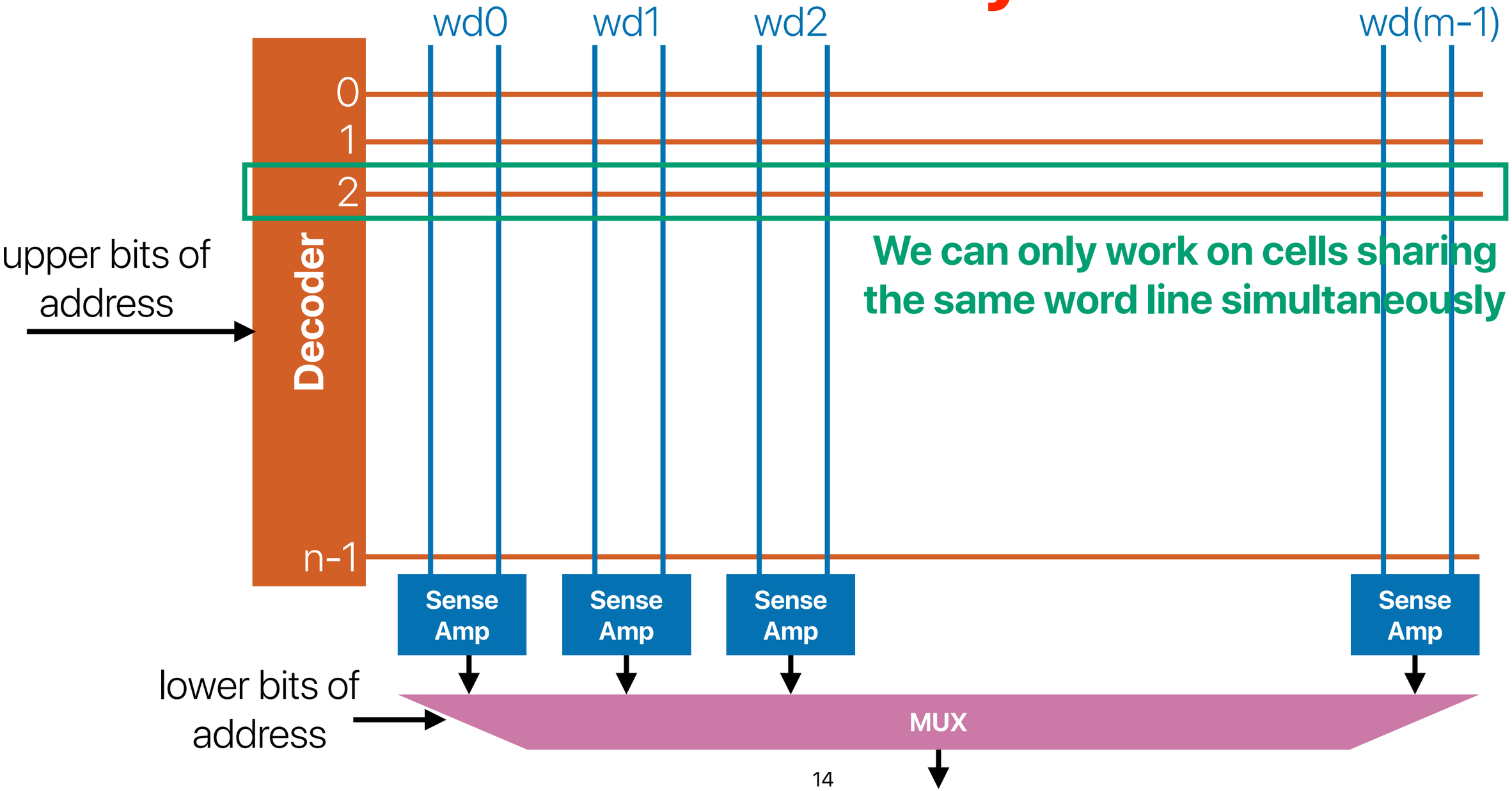
Write “0” to an SRAM Cell



Reading from an SRAM Cell

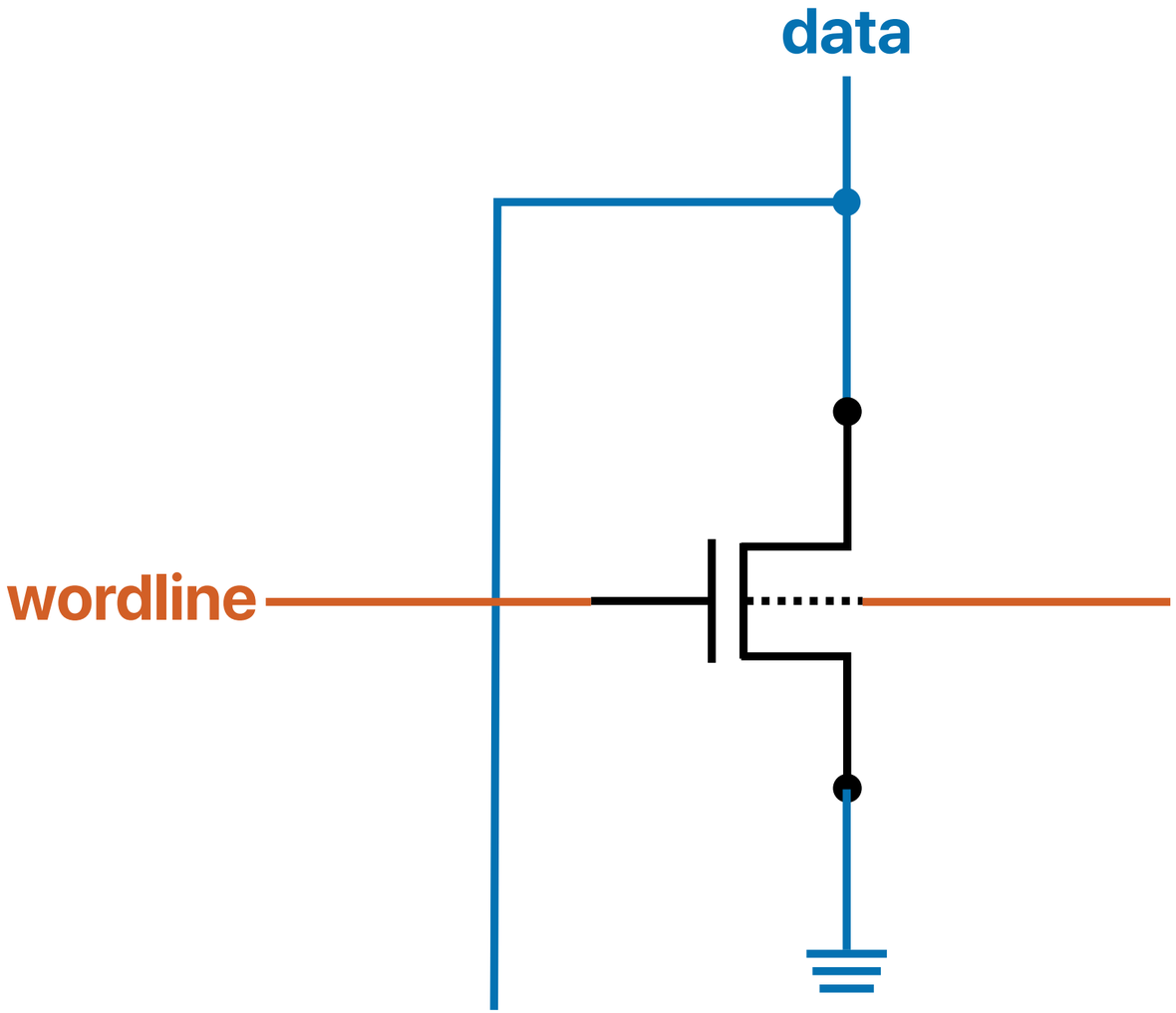


SRAM array


wd0
wd1
wd2
wd(m-1)
0
1
2
n-1
Decoder
upper bits of address
We can only work on cells sharing the same word line simultaneously
Sense Amp
Sense Amp
Sense Amp
Sense Amp
lower bits of address
MUX

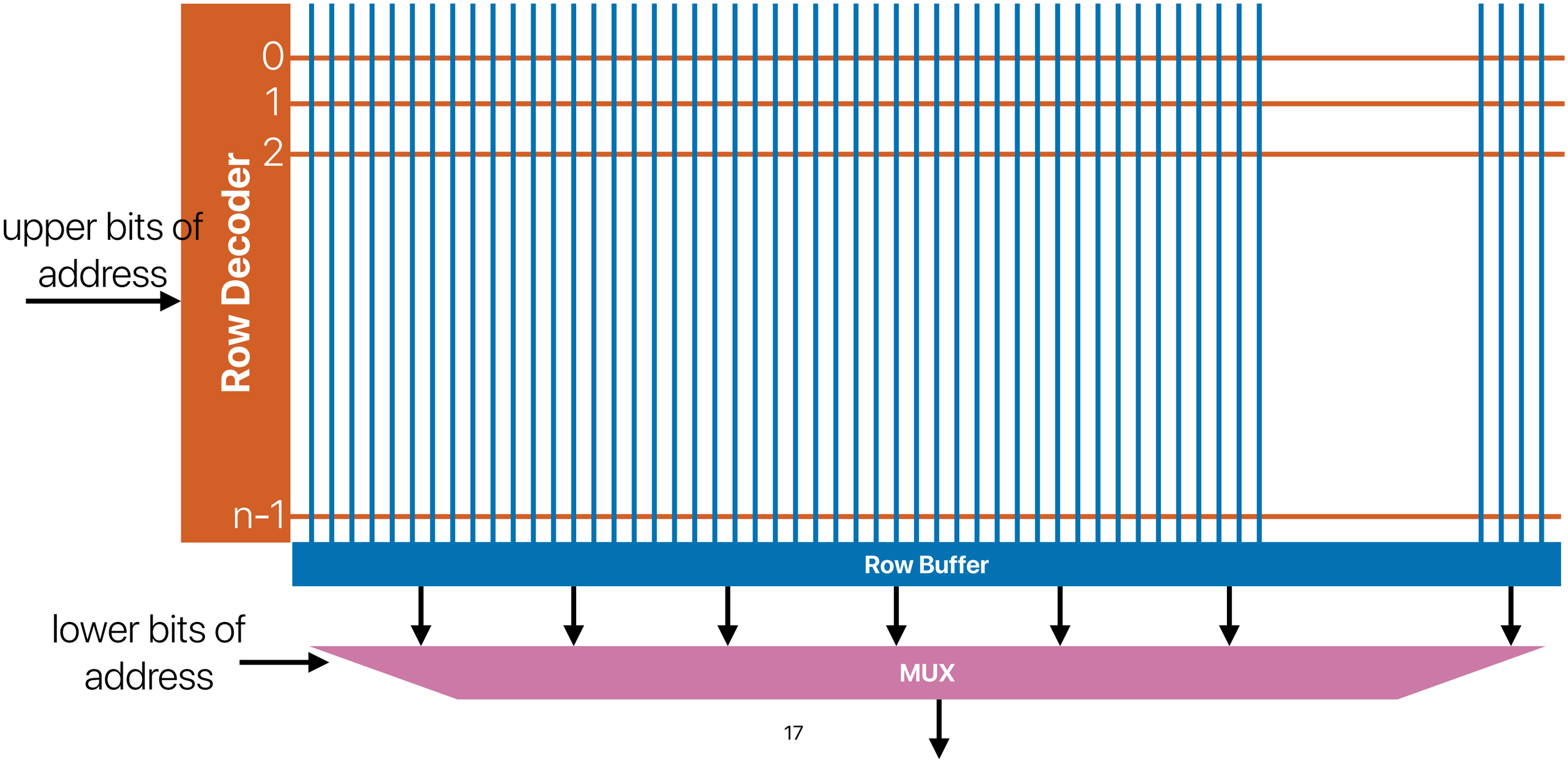
Dynamic Random Access Memory (DRAM)

An DRAM cell

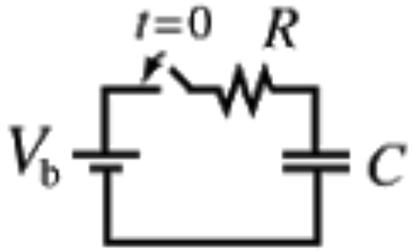


- 1 transistor (rather than 6)
- Relies on large capacitor to store bit
  - Write: transistor conducts, data voltage level gets stored on top plate of capacitor
  - Read: look at the value of d
- Problem: Capacitor discharges over time
  - Must “refresh” regularly, by reading d and then writing it right back

DRAM array


0
1
2
n-1
Row Decoder
upper bits of address
Row Buffer
lower bits of address
MUX

RC charging



$$V_b = V_R + V_C$$

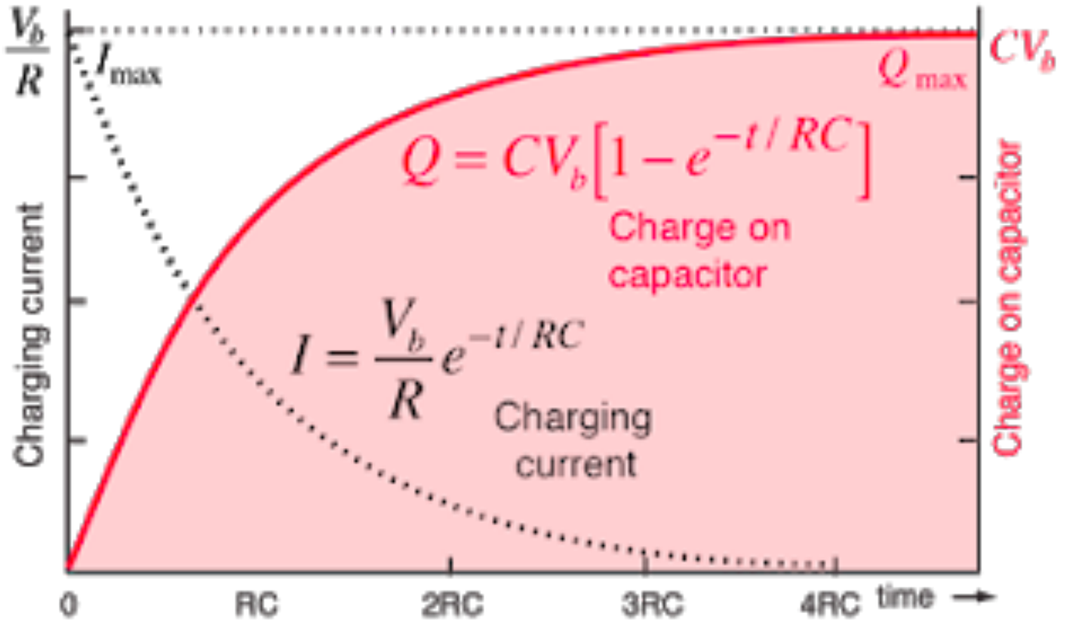
$$V_b = IR + \frac{Q}{C}$$

As charging progresses,

$$V_b = IR + \frac{Q}{C}$$

$\uparrow$ $\downarrow$

current decreases and charge increases.



At $t = 0$

$Q = 0$

$V_C = 0$

$I = \frac{V_b}{R}$

As $t \to \infty$

$Q \to CV_b$

$V_C \to V_b$

$I \to 0$

Latency of volatile memory

	Size (Transistors per bit)	Latency (ns)
Register	18T	~ 0.1 ns
SRAM	6T	~ 0.5 ns
DRAM	1T	50-100 ns

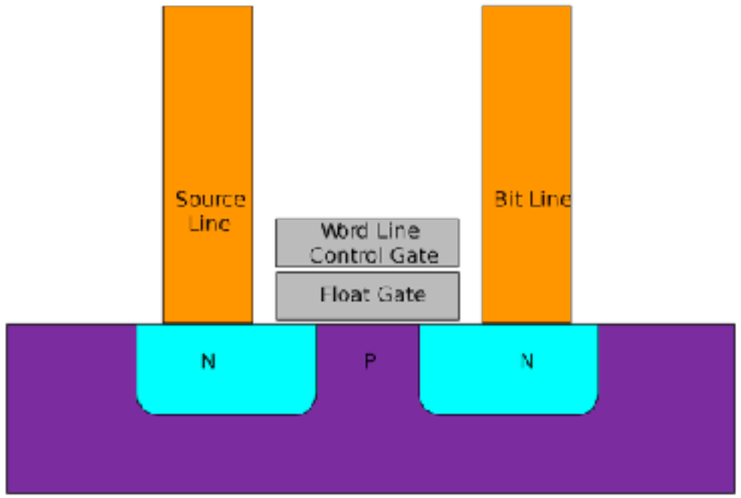
Non-volatile memory

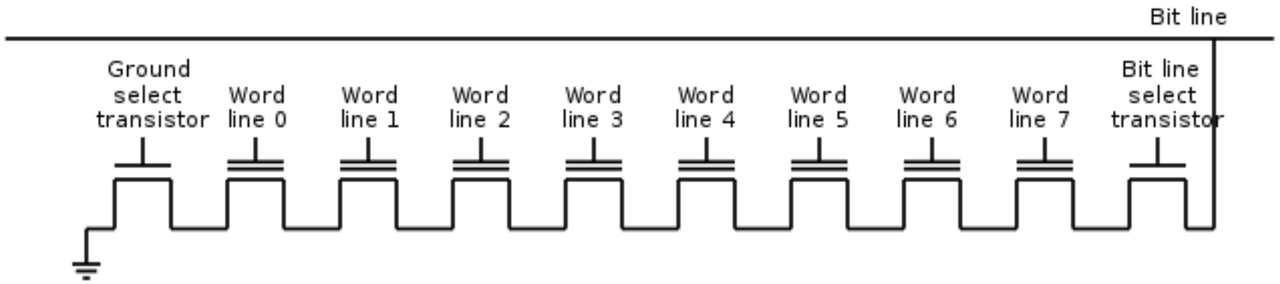
Volatile v.s. Non-volatile

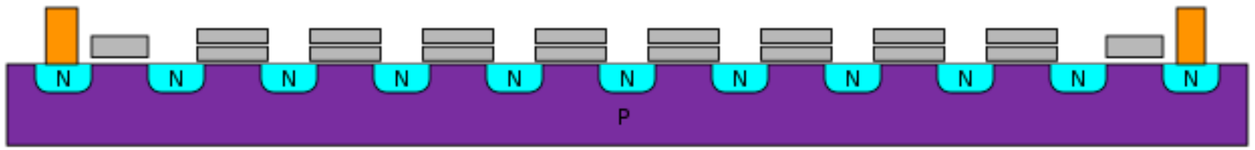
- Volatile memory
  - The stored bits will vanish if the cell is not supplied with eletricity
  - Register, SRAM, DRAM
- Non-volatile memory
  - The stored bits will not vanish “immediately” when it’s out of electricity — usually can last years
  - Flash memory, PCM, MRAM, STTRAM

Flash memory

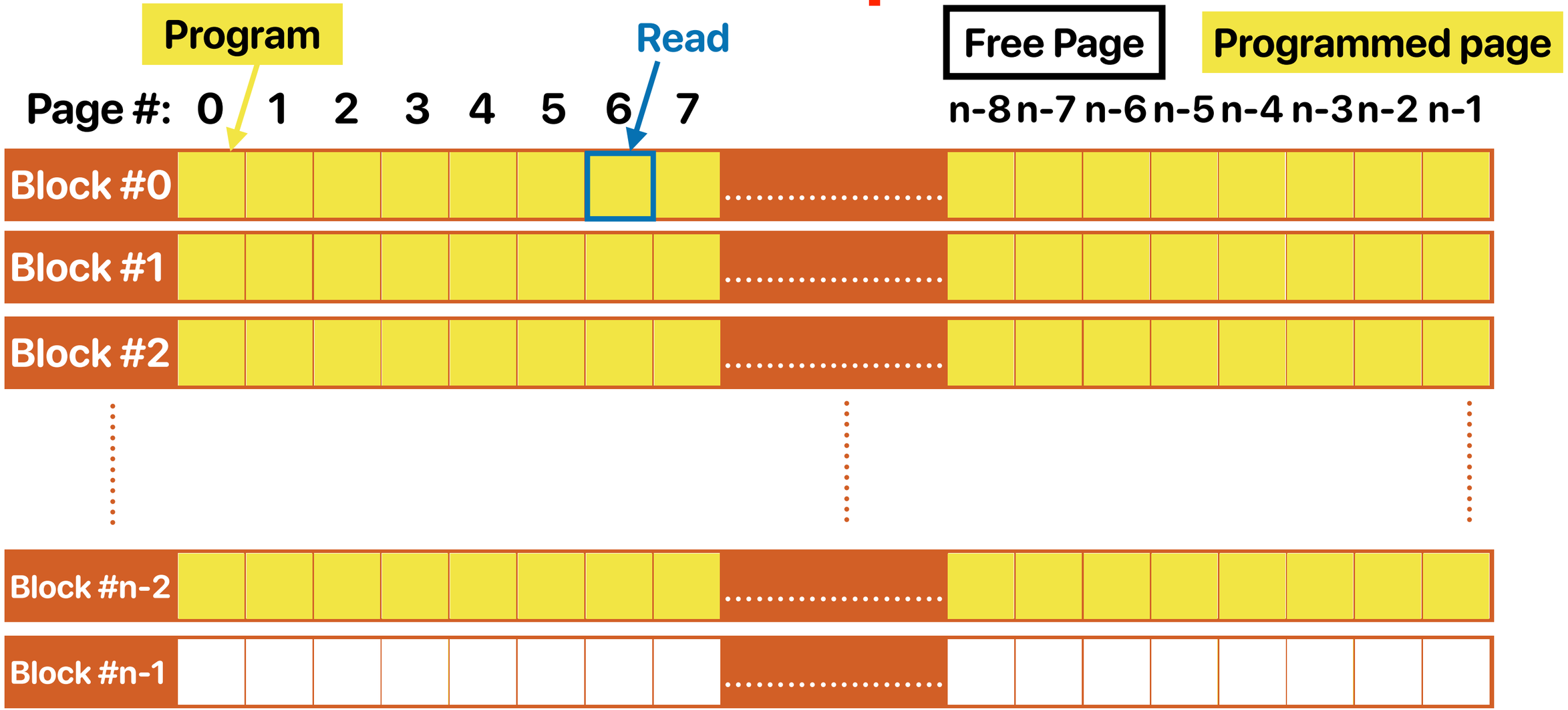
- Floating gate made by polycrystalline silicon trap electrons
- The voltage level within the floating gate determines the value of the cell
- The floating gates will wear out eventually







Basic flash operations

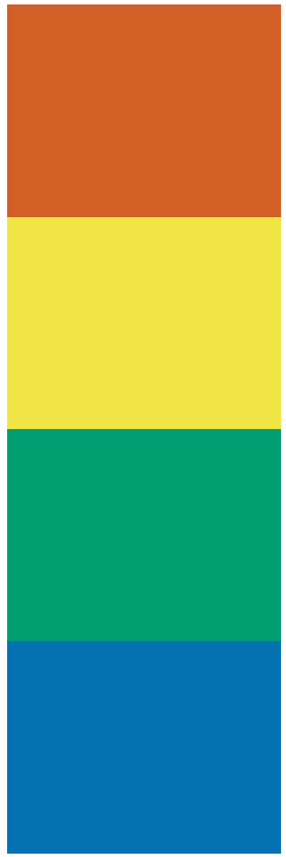


Types of Flash Chips

2 voltage levels, 1-bit

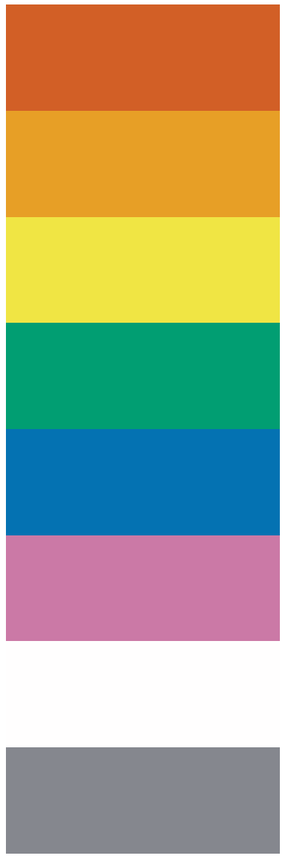
Single-Level Cell (SLC)

4 voltage levels, 2-bit



Multi-Level Cell (MLC)

8 voltage levels, 3-bit



Triple-Level Cell (TLC)

16 voltage levels, 4-bit

Quad-Level Cell (QLC)

Programming in MLC

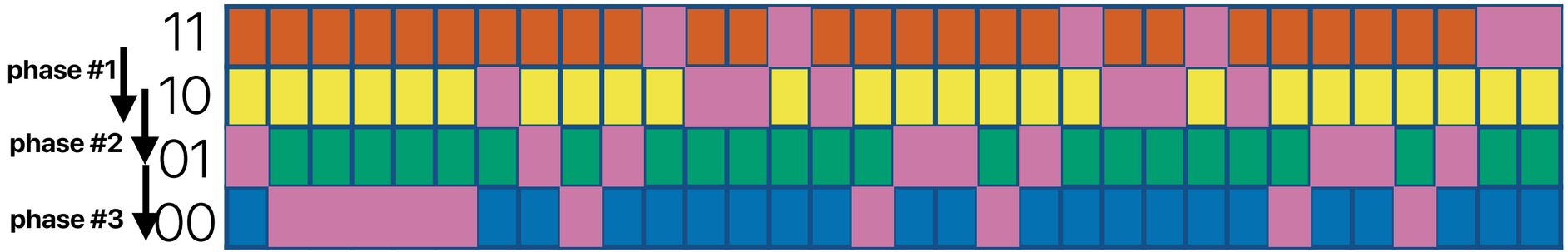
4 voltage levels,
2-bit

Multi-Level Cell (MLC)

3.14000000000000012434497875800

= 0x40091EB851EB851F

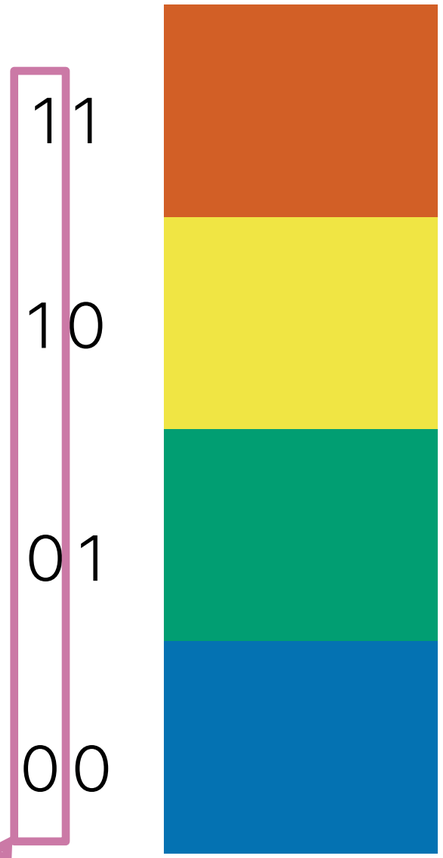
= 01000000 00001001 00011110 10111000 01010001 11101011 10000101 00011111



3 Cycles/Phases to finish programming

Programming in MLC

4 voltage levels,
2-bit



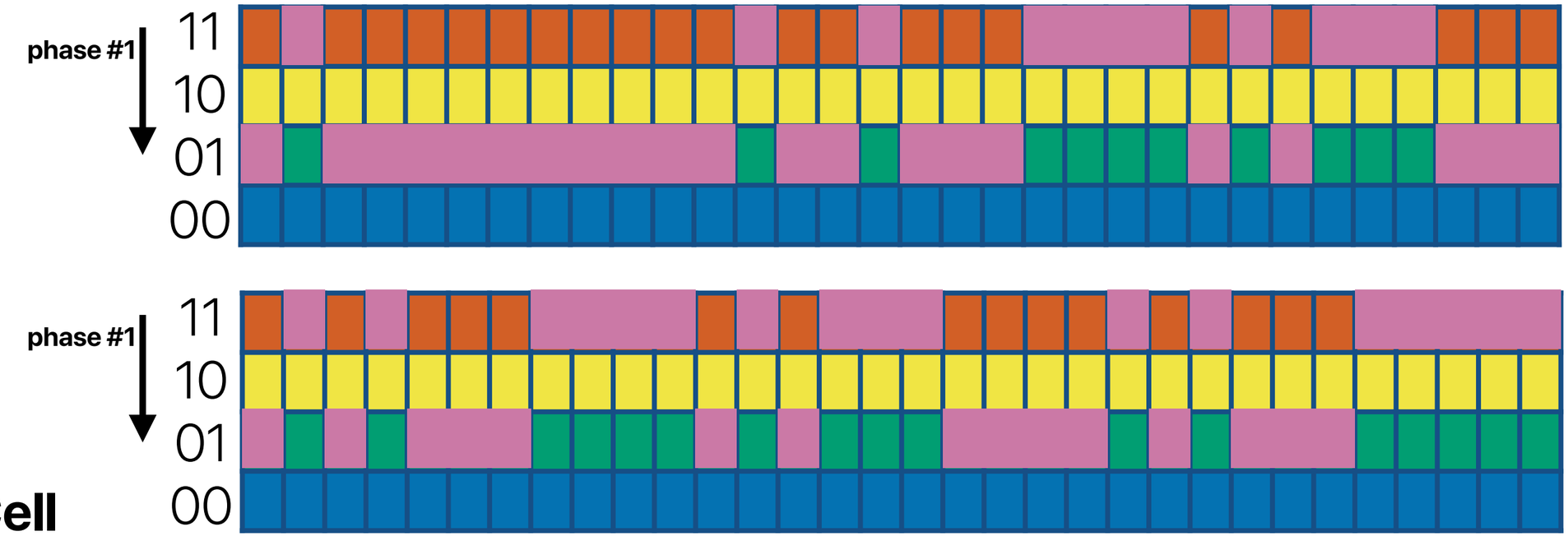
1st page

Multi-Level Cell (MLC)

3.14000000000000012434497875800

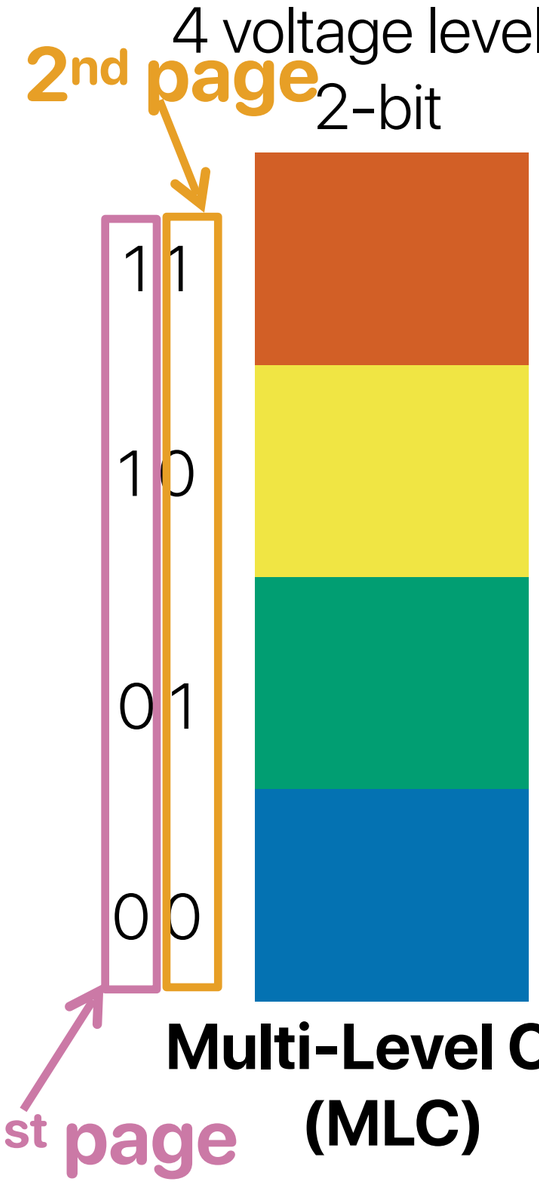
= 0x40091EB851EB851F

= 01000000 00001001 00011110 10111000 01010001 11101011 10000101 00011111



1 Phase to finish programming the first page!

Programming the 2nd page in MLC

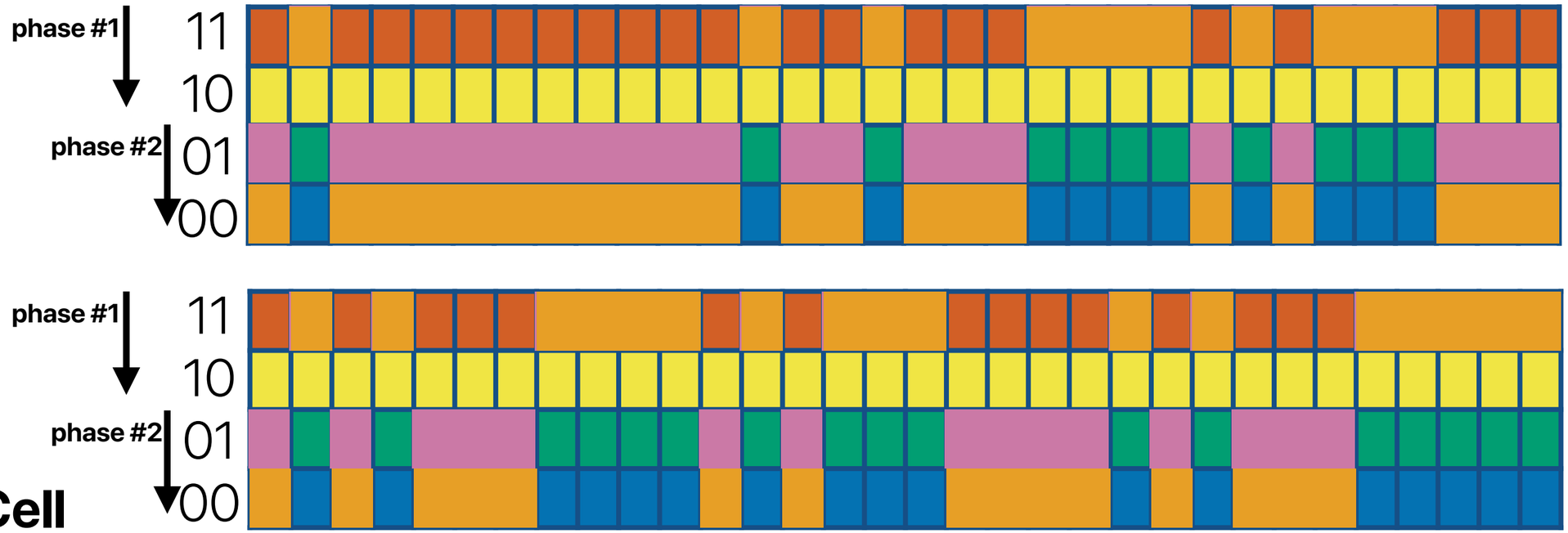


3.14000000000000012434497875800

= 0x40091EB851EB851F

= 01000000 00001001 00011110 10111000 01010001 11101011 10000101 00011111

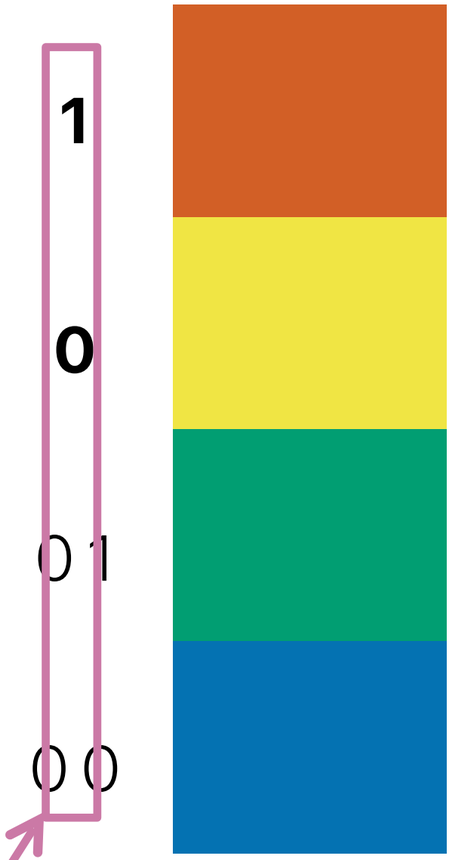
= 01000000 00001001 00011110 10111000 01010001 11101011 10000101 00011111



2 Phase to finish programming the second page!

Optimizing 1st Page Programming in MLC

4 voltage levels,
2-bit



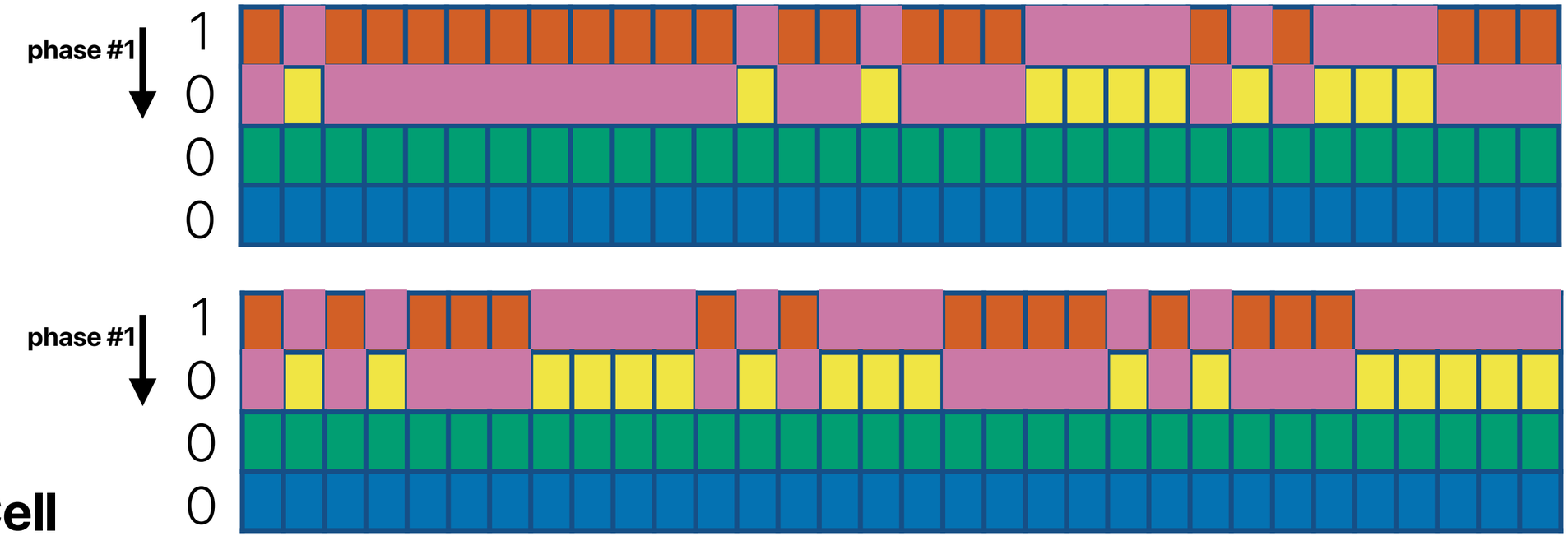
Multi-Level Cell (MLC)

1st page

3.14000000000000012434497875800

= 0x40091EB851EB851F

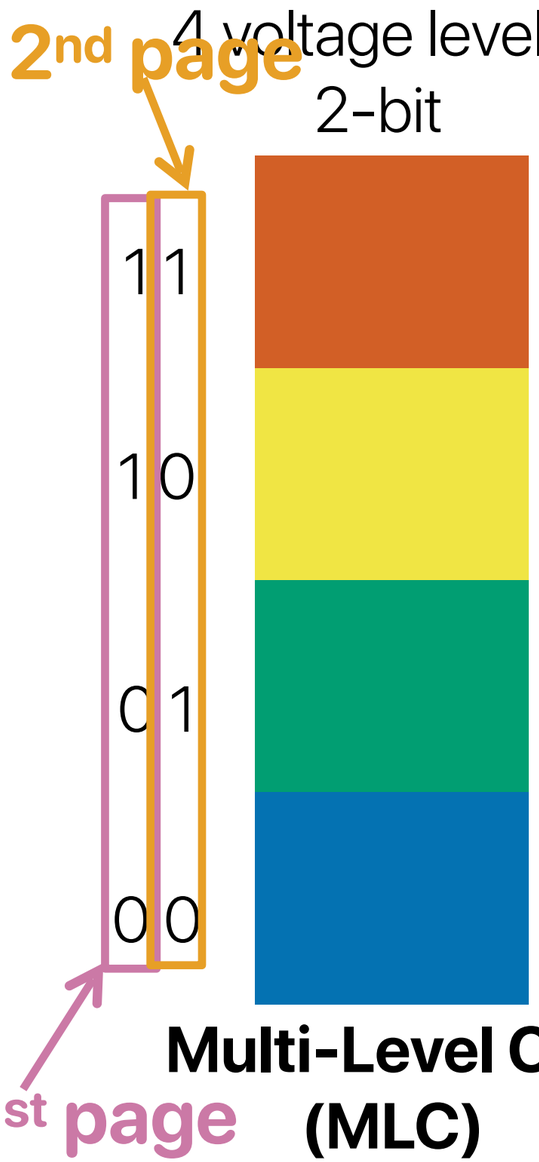
= 01000000 00001001 00011110 10111000 01010001 11101011 10000101 00011111



1 Phase to finish programming the first page!

— the phase is shorter now

2nd Page Programming in MLC

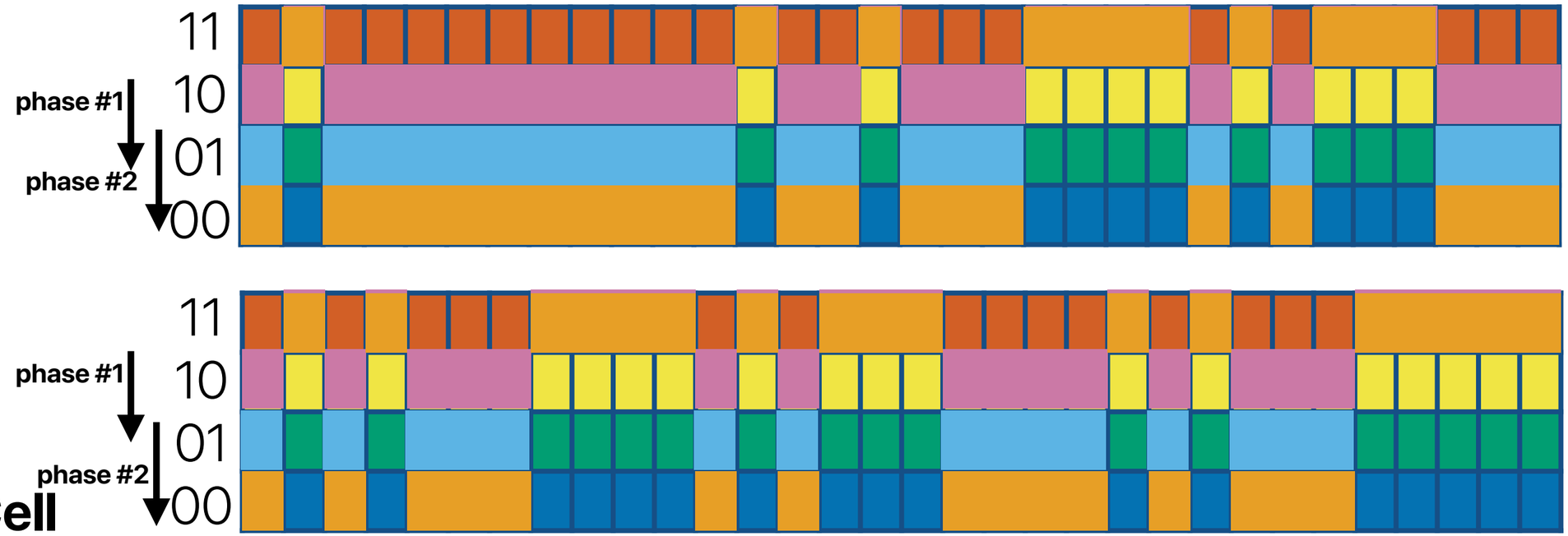


3.14000000000000012434497875800

= 0x40091EB851EB851F

= 01000000 00001001 00011110 10111000 01010001 11101011 10000101 00011111

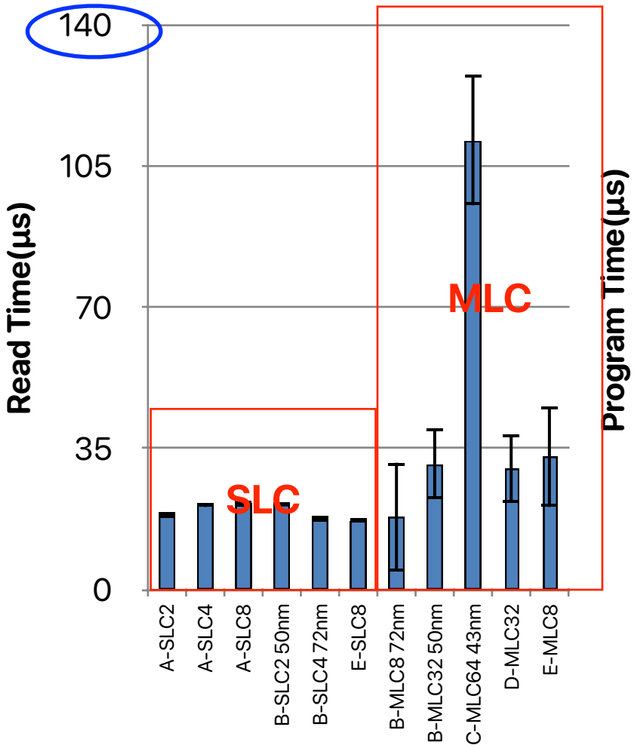
= 01000000 00001001 00011110 10111000 01010001 11101011 10000101 00011111



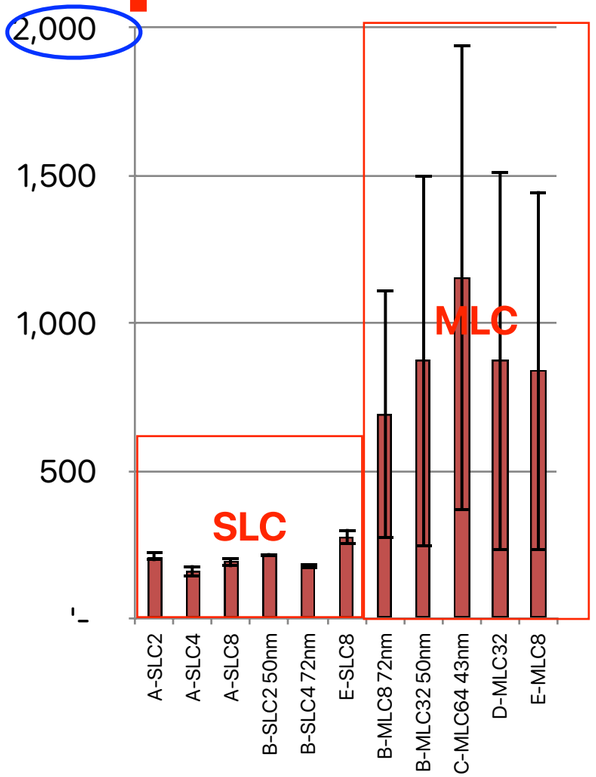
2 Phase to finish programming the second page!

Flash performance

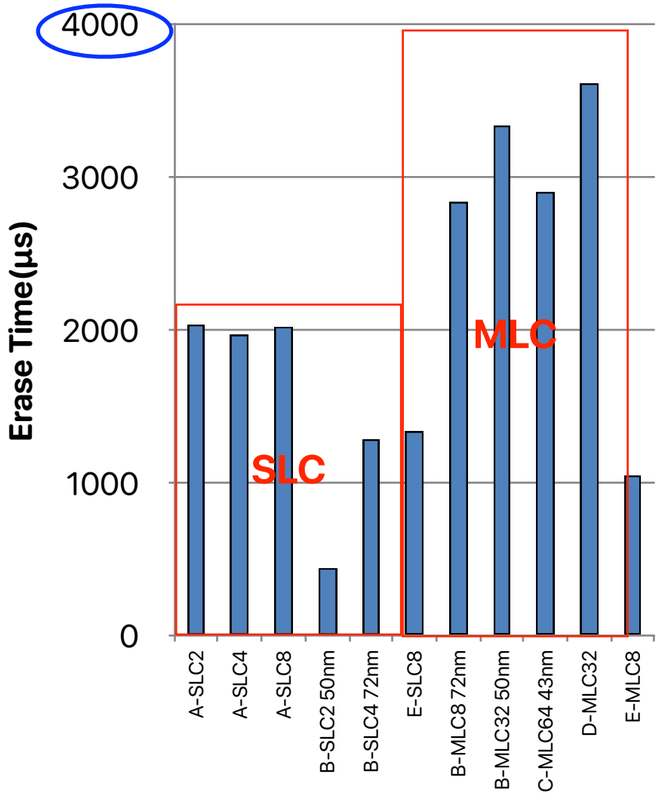
Not a good practice



Reads: less than 150us



Program/write: less than 2ms

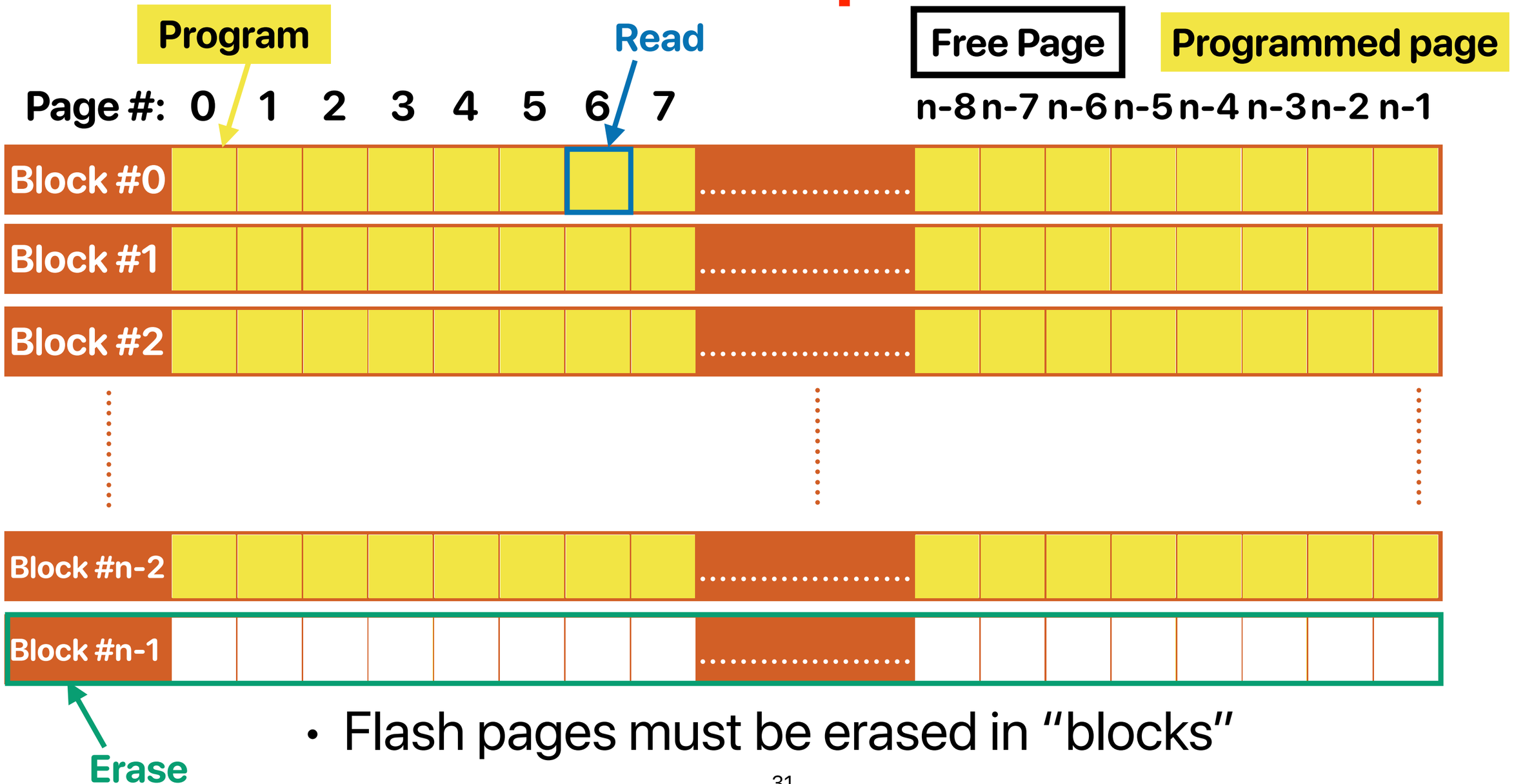


Erase: less than 3.6ms

Similar relative performance for reads, writes and erases

Laura M. Grupp, Adrian M. Caulfield, Joel Coburn, Steven Swanson, Eitan Yaakobi, Paul H. Siegel, and Jack K. Wolf. Characterizing flash memory: anomalies, observations, and applications. In MICRO 2009.

Basic flash operations



- Flash pages must be erased in “blocks”

If programmer doesn't know flash "features"

- Software designer should be aware of the characteristics of underlying hardware components

Spotify is writing massive amounts of junk data to storage drives

Streaming app used by 40 million writes hundreds of gigabytes per day.

DAN GOODIN - 11/10/2016, 7:00 PM

Enlarge / SSD modules like this one are being abused by Spotify.

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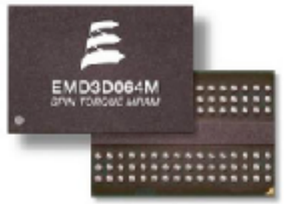
For almost five months—possibly longer—the Spotify music streaming app has been assaulting users' storage devices with enough data to potentially take years off their expected lifespans. Reports of tens or in some cases hundreds of gigabytes being written in an hour aren't uncommon, and occasionally the recorded amounts are measured in terabytes. The overload happens even when Spotify is idle and isn't storing any songs locally.

Non-volatile memory technologies



	H.D.D	Flash	Optane	STT-MRAM
Latency	~ 10-15 ms	~ 100 us (read) ~ 1 ms (write)	7 us (read) 18 us (write)	35 ns
Bandwidth	~200 MB/Sec	3.5 GB/sec (read) 2.1 GB/sec (write)	1.35 GB/sec (read) 290 MB/sec (write)	
Dollar/GB	0.0295	0.583	2.18	

Flash is still the most convincing technology for now

Announcement

- Assignment #4 due next Tuesday — **Chapter 4.8-4.9 & 5.2-5.4**
- Lab 5 is up — due next Thursday
  - Start early & plan your time carefully
  - Watch the video and read the instruction BEFORE your session
  - There are links on both course webpage and iLearn lab section
  - Submit through iLearn > Labs
- Check your grades in iLearn

Electrical
Computer Science
Engineering

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