UNIVERSITY OF CALIFORNIA, RIVERSIDE

Winter 2018

EE 100B ELECTRONIC CIRCUITS II

Instructor: Prof. Alexander Korotkov, 827-2345, korotkov@ee.ucr.edu
Office Hours: Wednesday, 3:00 pm – 4 pm, CHUNG 434

TAs: Feilong Zhang, fzhan008@ucr.edu, Office Hours: TBA, CHUNG 109 (TA room)
Howard Chiang, hchia002@ucr.edu, Office Hours: TBA

Lecture: Monday, Wednesday, Friday, 1:10 pm – 2:00 pm, CHUNG 143,
Labs: (021) Tuesday, 3:10 pm – 6:00 pm, (022) Wednesday, 6:10 pm – 9:00 pm,
(023) Thursday, 11:10 pm – 2:00 pm, CHUNG 128
(Lab orientation on Jan. 16, 17, 18, first lab on Jan. 23, 24, 25)

Final exam: Wednesday, 03/21/2018, 8:00 am to 11:00 am

Objective: This course is a continuation of EE 100A. The objective of this course is the further development of the ability to analyze and design electronic circuits. The emphasis is on analog circuits.

Text: *Microelectronic Circuits,* 7th edition, A. S. Sedra and K.C. Smith, Oxford University Press.

Laboratory Experiments: There will be seven (or six) experiments. A lab report is required for each experiment. The lab report is due one week after the scheduled date for the experiment.

Homework Assignments: There will normally be one homework assignment every week, due on the same day of the following week. One late assignment can be accepted within one week after its due date. The second late assignment (not more than 1 week late) receives 50% of the score. Any other late assignments are not accepted and not graded.

Exams: There will be one midterm and one final exam. The date of the midterm exam will be announced one week in advance. Short quizzes may be given occasionally; the grades for the quizzes are included into overall homework grading.

Grades: 10% assignments, 25% laboratory, 25% midterm, and 40% final exam.

Course Contents:

Building Blocks of IC amplifiers (Chapter 8)
Differential and multistate amplifiers (Chapter 9)
Feedback (Chapter 11, Secs. 11.1–11.7)
Output stages (Chapter 12, Secs. 12.1–12.7)
Signal generators and waveform-shaping circuits (Chapter 18, Secs. 18.1–11.6)
Filters (selected material from Chapter 17, if time permits)
Frequency response (selected material from Chapter 10, if time permits)
CMOS digital logic circuits (Chapter 14)
Memory circuits (selected material from Chapter 16)