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Single-electron logic and memory devices

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Single-electronics is believed to be the leading candidate for future digital electronics which will be able to operate at ~ 10 nm size scale and below. However, the problems of integrated single-electronics are quite serious whereby the future prospects are still uncertain. In this paper we discuss the operation principles and required parameters of several proposed families of single-electron logic, including the logic based on single-electron transistors, wireless single-electron logic and single-electron parametron. We also briefly discuss the single-electron memory which is easier to implement than logic and, hence, is more important from the practical point of view. As an example, we consider the background-charge-insensitive hybrid SET/FET memory.

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1. Introduction

More than 10 years has past since the beginning of the active theoretical and experimental study of correlated single-electron tunnelling (for reviews see, e.g. [1–6]). This is already a sufficiently long period of time to ask a question if the applied single-electronics is only a dream or we can expect the creation of really useful single-electron devices in the not too distant future. However, there is still no simple answer to this question. On the one hand, the practical value of several non-integrated applications have been already proven. On the other hand, for the integrated digital single-electron devices which are the most important potential application of single-electronics, the prospects are still not so clear.

Among the definitely practical applications of single-electronics let us first of all mention the use of the single-electron transistor [7–9] (SET-transistor or SET) as a very sensitive electrometer. At present this is the only device which is able to measure reliably the subelectron charges. A sensitivity better than $10^{-4}\, e\,\mathrm{Hz}^{-1/2}$ (at 10 Hz) has already been achieved [10, 11] experimentally, and a sensitivity of about $10^{-6}\, e\,\mathrm{Hz}^{-1/2}$ is expected to be achieved soon in the $\sim 10^5$ Hz frequency range. Let us also mention the fabrication of the scanning SET microscope [12] which can become a useful tool for surface characterization.

Another clear application of single-electronics is the single-electron standard of dc current [1]. Initially there was an attempt to use the synchronization between single-electron oscillations in the array of junctions and external rf field for this purpose [13]. It was shown later that the single-electron pump [14] is much more suitable for a dc current standard. At present the relative accuracy of about 10^{-8} has been achieved [15] for the prototype of such a device. A similar device can also be used for the standard of capacitance.

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Another interesting application of single-electronics is the absolute thermometer for low temperatures using the array of junctions [16]. An accuracy of about 1% has been achieved experimentally [17].

So, there is confidence that at least several analogue applications of single-electronics will be really useful. Unfortunately, there is no such confidence so far about the digital single electron devices. There are two main reasons why this task is much more complicated. First, real digital devices should operate at room temperature (or at least at 77 K) while for the applications mentioned above a much lower temperature is acceptable. The increase of the operation temperature is still the most important and most difficult problem of single-electronics. Second, digital devices should be suitable for the integration at very large scale. This creates difficult technological problems (reproducibility, etc.) as well as physical questions (for example, the problem of the background charge fluctuations).

However, despite the difficulties, there is fast experimental progress in the area related to digital single-electronics. Single-electron transistors operating at temperatures higher than 77 K and even at room temperature have been demonstrated using a variety of materials [18–23] proving the possibility of room temperature single-electronics. The controllable trapping of single electrons have also been demonstrated using different materials and technologies including the 'standard' aluminium double-angle technique [24–26], GaAs structures [27], and Si-based structures [28–32]. The multi-electron memory cell with the readout by a single-electron transistor operating in a background-charge-insensitive mode has recently been reported in [33].

There are two main possible areas of prospective digital single-electronics: logic and memory devices. There have been many theoretical suggestions of different kinds of single-electron logic (see, e.g. [8, 34–50]) and only a few theoretical proposals for the single-electron memory (see, e.g. [51]). In the present-day understanding, the single-electron logic is much more difficult for experimental implementation than memory devices. Nevertheless, the practical importance of ultradense logic circuits makes the study of different possibilities of such devices very meaningful.

In this paper we will discuss several theoretical suggestions for both single-electron logic and memory devices concentrating on the logic. After the brief review of the basic physics of single-electron tunnelling we will consider first the logic circuits based on SET-transistors [8, 34–36]. Then we will discuss the principles of the so-called SEL logic [37–40] in which the digital bits are represented directly by single electrons, and two specific kinds of this logic: wireless single-electron logic [43] and single-electron parametron [44, 45]. After that we will consider the single-electron memory, compare advantages and disadvantages of the memory cells based on the storage of one or few electrons, and discuss the proposal of the background-charge-insensitive single-electron memory. In conclusion the general prospects of digital single-electronics will be discussed.

2. Basic physics of single-electron tunnelling

2.1. *Orthodox theory*

The single-electron devices are based on the correlated tunnelling [1] of single electrons in the systems of small tunnel junctions. If the capacitance C of a junction is sufficiently small, then the difference $V_b - V_a = e/C$ between the voltages across

the junction before and after tunnelling of a single electron is sufficiently large to produce noticeable effects.

In order not to smear this voltage difference, the quantum fluctuations of the charge should be sufficiently small, which requires a sufficiently large tunnel resistance R

$$R \gg R_Q = \pi\hbar/2e^2 \simeq 6.5\,\mathrm{k}\Omega \quad (1)$$

To avoid the smearing of single-electron effects by thermal fluctuations, the thermal energy T (we use $k_B = 1$) should be much less then the typical one-electron charging energy

$$T \ll e^2/2C \quad (2)$$

(Note that in the system of junctions the capacitance C should be replaced by the effective junction capacitance which takes into account the rest of the circuit.) As a numerical example, for $C = 10^{-18}$ F the charging energy $e^2/2C \simeq 80\,\mathrm{meV} \simeq 930\,\mathrm{K}$.

Most of the single-electron experiments can be quantitatively described by the simple 'orthodox' theory [1, 52] which is valid when condition (1) is well satisfied. In this theory the effective voltage for the electron tunnelling is just the average between the voltages before and after tunnelling

$$V_{\mathrm{eff}} = (V_b + V_a)/2 \quad (3)$$

and the tunnelling rate Γ is given by the expression

$$\Gamma = \frac{V_{\mathrm{eff}}}{eR[1 - \exp(-eV_{\mathrm{eff}}/T)]} \quad (4)$$

(This equation can be easily modified for the nonlinear 'seed' I–V curve of the tunnel junction [1].) The orthodox theory neglects the higher order quantum effects and considers the transport as the sequential jumps of 'classical' electrons with the tunnelling rates changing after each jump.

The simplest experimental realization of a single-electron circuit consists of two tunnel junctions in series [figure 1(*a*)] [8]. The I–V curve of this system exhibits the region of Coulomb blockade at small bias voltages V: the tunnelling is blocked when V is not sufficient to provide the energy for single-electron charging of the central

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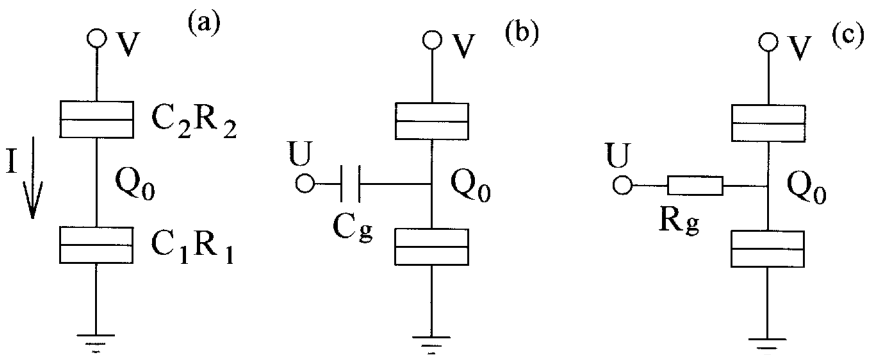

Figure 1. Single-electron transistor (SET): (*a*) the basic part consisting of two tunnel junctions in series, (*b*) capacitively coupled SET (C-SET), and (*c*) resistively-coupled SET (R-SET).

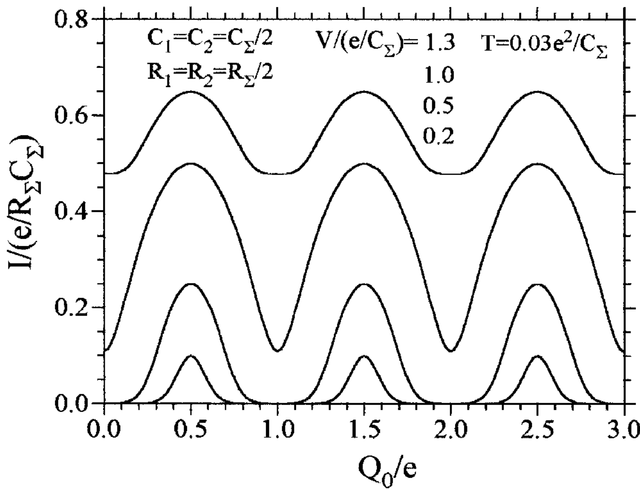

Figure 2. The typical theoretical dependence of the current through the symmetrical SET-transistor on the induced charge Q_0 for different bias voltages V.

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island. If the two tunnel resistances are considerably different, then the I–V curve shows also the step-like structure (called the Coulomb staircase), with each next step corresponding to one more electron on the central island. Finally, the most important feature of the double-junction system is the e-periodic dependence (called Coulomb oscillations) of the current I on the background charge Q_0 of the central island (figure 2). Very high (subelectron) sensitivity to the charge of the central island is the basis of the SET-transistor operation. Controlling Q_0 by a capacitively coupled gate [C-SET, figure 1(*b*)] or via a coupling resistor [R-SET, figure 1(*c*)], allows one to control the flow of electrons through the SET-transistor.

R-SET is quite difficult to implement because the coupling resistance R_g should be much larger than R_Q to prevent quantum fluctuations of Q_0; simultaneously the resistor size should be sufficiently small so that its stray capacitance does not significantly increase the total island capacitance C_Σ. Experimental demonstration of the R-SET is still a difficult problem despite significant progress in this direction [53–55].

In contrast, C-SET was demonstrated repeatedly by many scientific groups using different materials and technologies (the first experiments [9, 56] were reported in 1987). The gate voltage U [see figure 1(*b*)] induces the effective charge into the central island, $Q_0 \to Q_0 + C_g U$ (C_g is the gate capacitance), hence figure 2 can also be considered as a control curve of the C-SET (the gate voltage period is equal to $\Delta U = e/C_g$).

2.2. *Fluctuations*

At present the majority of experiments with SET-transistor are done at relatively low frequencies (less than 1 kHz), and in this case the charge sensitivity is usually limited by $1/f$ noise caused by fluctuating impurities which induce the fluctuating background charge. At frequencies above $\sim 10^5$ Hz (for typical present-day technology) the contribution from $1/f$ should become negligible in comparison with the shot noise caused by the randomness of the tunnelling process.

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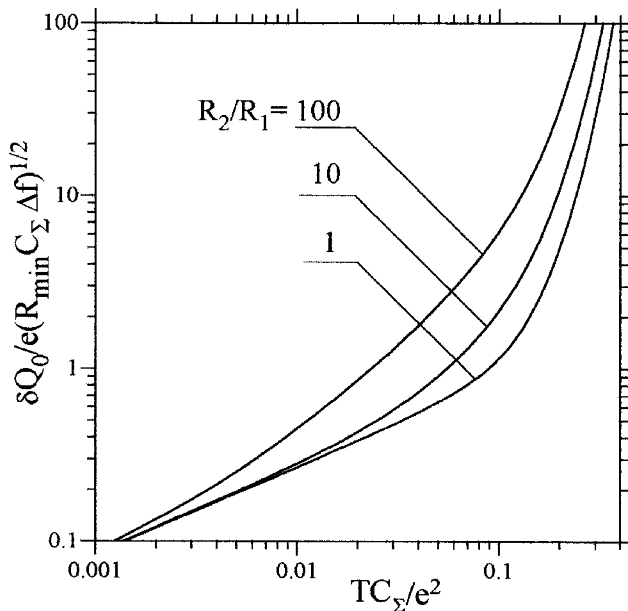

Figure 3. The ultimate sensitivity of SET-transistor limited by the shot noise as a function of the temperature [58].

There are two methods of the shot noise calculation for SET-transistor both giving the same result (one method is based on the Fokker–Plank approach [57–59] while the other uses the quasi-Langevin technique [60]). The very crude estimate of the shot noise can be given by the Schottky formula $S_I = 2eI$. However, the noise can be slightly lower than this level at small temperatures or higher (may be much higher) at relatively large temperatures. The shot noise limits the ultimate sensitivity of the SET-transistor. Figure 3 shows the minimum detectable charge δQ_0 of the central electrode of C-SET for the given bandwidth Δf, as a function of temperature for different ratios of tunnel resistances R_1 and R_2. At low temperatures the dependence scales as $T^{1/2}$ while the sensitivity starts to worsen rapidly at $T \gtrsim 0.1e^2/C_\Sigma$ (where $C_\Sigma = C_1 + C_2 + C_g$).

For the typical present-day 'low-temperature' aluminium technology $C_\Sigma \simeq 2 \times 10^{-16}$ F, so for $R \simeq 10^5\,\Omega$ and $T \simeq 0.1$ K one can obtain from figure 3 the ultimate sensitivity $1.3 \times 10^{-6}\,e\,\mathrm{Hz}^{-1/2}$. For the 'highest-temperature' technology with $C_\Sigma \simeq 10^{-18}$ F and $R \simeq 10^5\,\Omega$, the lower curve of figure 3 gives the similar value about $9 \times 10^{-7}\,e\,\mathrm{Hz}^{-1/2}$ at $T = 300$ K. This means that assuming the coupling to the signal source to be about 0.1, one electron charge can be reliably determined by the SET-transistor operating at a frequency up to 10^{10} Hz.

At even higher frequencies the quantum noise of the device becomes important [60, 61]. However, it is not likely to be essential for practical devices.

2.3. *Cotunnelling*

The orthodox theory considers only one-electron tunnelling events. So, there is no tunnelling at all within the range of Coulomb blockade at sufficiently low temperatures. However, that is only an approximation. The 'quantum' many-electron

transport is possible via classically forbidden intermediate states. For example, if in a SET transistor two electrons tunnel 'simultaneously' through both tunnel junctions (cotunnelling), then the total energy gain is always positive for non-zero bias voltage. Hence, such two-electron processes are always possible, and they provide the current within the Coulomb blockade range.

The rate of n-electron cotunnelling process scales as R^{-n} [62, 63] with the increase of tunnel resistance R, so cotunnelling is especially important for relatively low R (when it becomes comparable to R_Q).

Even the basic theory of cotunnelling [62, 63] leads to rather time-consuming calculations for the rates of n-order cotunnelling events if $n \gtrsim 5$, so some simplifications [64] are useful. The rate given by the basic theory diverges when the process of lower order becomes possible and, hence, this approximation is not able to consider the coexistence of the cotunnelling of different orders. Nevertheless, slight modification allows the use of this approximation in the computer code which can treat arbitrary cotunnelling processes [65] in logic/memory devices. Further development of the theory of cotunnelling beyond the basic approximation is quite significant (see, e.g. [57, 66–70]). However, these theories still can hardly be used for acceptably fast numerical calculations of high-order cotunnelling in complex single-electron systems.

Notice that processes of cotunnelling are especially important for logic and memory devices in which the digital bits are represented by single electrons and, hence, one cotunnelling event can be sufficient to destroy the digital information.

2.4. *Room-temperature single-electronics*

The room temperature applications of single-electronics require extremely small capacitances and, hence, very small typical size of the conducting islands. This size should not be larger than a few nm and quite possibly it can be below the 1 nm mark if the prospects of molecular electronics are to be realized. At this size scale new effects, different from that considered in orthodox theory, necessarily become important. Here we will briefly discuss two of them: the level discreteness and the barrier suppression by applied voltage.

While the self capacitance of a conducting island scales linearly with the island dimension d, the energy difference between neighbouring quantized energy levels scales as d^{-2} in the 2D case and as d^{-3} in the 3D case for fixed concentration of conducting electrons (the energy spacing between the first few quantized levels scales as d^{-2} in the 3D case as well). Hence, at sufficiently small d this energy difference becomes comparable to the typical single-electron energy $e^2/2C$ (the junction capacitances are on the order of self-capacitances at few-nm size scale). In 2D structures this occurs when d becomes comparable to the Bohr radius [71] (a similar condition applies for 3D semiconductor islands with few-electron charging), in 3D many-electron structures it depends on the electron (or hole) concentration, so that in semiconductors this occurs at considerably larger d than in metals.

The theory of single-electron tunnelling should be modified to take into account the level discreteness, and it can be done in a similar way for metal clusters [72] and semiconductor quantum dots [71, 73]. The main difference from the orthodox theory is that the energy of a particular electron distribution among the discrete levels should be added to the electrostatic energy. (At even smaller size scale the distinction between these two kinds of energy becomes useless and the total energy should be calculated for each state individually similar to atomic physics.)

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The I–V curve of the SET-transistor with the discrete energy spectrum of the central island consists of steps [71–72], each of them corresponding to some discrete energy level crossing the Fermi level in the electrode (this can occur at different charging of the island, so many series of steps are possible). The Coulomb staircase as well as the Coulomb oscillations are no longer periodic because of the contribution from the energy difference δ between discrete levels.

It is important that the SET-transistor with discrete levels can operate at somewhat higher temperature than in the orthodox case, because crudely in equation (2) the energy δ should be added to the single-electron charging energy. However, the disadvantage is a typically random distribution of energy levels which leads to some randomness in the transistor characteristics.

The second issue which is necessarily important for room-temperature single-electronics, is the fact that the Coulomb energy can become comparable to the height of the tunnel barrier. In this case the I–V curve of the SET-transistor acquires the exponential overall shape [74] because of the suppression of the tunnel barrier by the voltage across the junction. (If the nonlinearity is sufficiently large, the contribution from the single-electron image charge [75, 76] should be taken into account, but this effect is not likely to be important for practical devices.) The relatively low tunnel barriers can lead to serious difficulties for room temperature single-electronics [77]. However, this problem is definitely not the main problem on the way to digital devices.

Let us mention one more effect which is important in semiconductor single-electron devices. In contrast to metallic systems, the geometrical size of the conducting core of a semiconductor island can depend on the number of electrons on the island and on the gate voltage. (The conducting core is typically smaller than the nominal size of an island; even the very formation of an island can be directly determined by the applied electric field as in the split-gate technique.) Because of the size variation, the capacitance is not constant, leading to non-periodicity of the Coulomb staircase and non-periodic dependence on the gate voltage in a SET-transistor. The change of geometric size also leads to the change of width of a tunnel barrier while the barrier height can be directly affected by the gate voltage. Sufficiently large gate voltage can either completely deplete the conducting island or remove the tunnel barrier depending on the polarity. As a consequence, on the large scale of the gate voltage semiconductor SET-transistors usually behave like field effect transistors (FETs): starting from the state with negligible current, one can finish with the perfectly open transport channel. The Coulomb oscillations in this case are observed only in the range of the gate voltage when the conducting island has already appeared and the tunnel transport has become possible, but the tunnel resistance of the barrier is still larger than the quantum unit R_Q.

Concluding this section, let us briefly mention the corrections to the orthodox theory due to electromagnetic environment [78, 79] and the possibility of the overheating of the electron gas due to tunnelling [80, 81] that can be important in applications.

3. Logic circuits based on SET-transistors

The most straightforward idea of digital single-electronics is the use of the SET-transistor as an active element instead of the FET. The circuit design in this case is similar to the conventional electronics while some difference should arise because of

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the different features of SETs and FETs. The digital information is conventionally represented by the voltage levels of the wires interconnecting the logic gates. The corresponding load capacitance is relatively large so that many electrons (on the order of 10^2 or more as we will discuss later) should be moved to or from the load capacitance to change the digital level. So, the single-electron effects are used only for the operation of SETs while the circuit architecture is almost traditional.

Let us emphasize that this is not the only possible idea. The alternative is the representation of the digital bits directly by single electrons so that, for example, the presence of an extra electron on the conducting island corresponds to digital unity while its absence corresponds to digital zero. This type of logic (usually called SEL-logic) does not use SET-transistors and has obvious advantages in the speed and power consumption in comparison with the SET-based logic. However, it is much less robust and more difficult to implement. We will discuss SEL-logic in the following sections while in this section we consider the logic based on SET-transistors.

The characteristics of the SET-transistor (we consider here the C-SET) are quite different from that of the FET. One main difference is the periodic dependence on the gate voltage for the SET instead of monotonous dependence for the FET. This requires more strictly controlled gate voltages in SET-based logic because too low or too high voltage level can produce the opposite response. Alternatively, this feature allows complementary circuits made of physically identical transistors. The second main difference is the relatively small voltage gain of the SET (while the dc power amplification is formally infinite because of zero dc input current). The voltage gain $K_V = |dV_{out}/dV_{in}|$ is limited [8] by the inequality

$$K_V \leq C_g/\min(C_1, C_2) \qquad (5)$$

and it is further reduced at finite temperature. The condition $K_V > 1$ which is necessary for the operation of logic devices requires the gate capacitance C_g to be larger than the junction capacitance. Such transistors have been demonstrated experimentally [10, 82] (in the majority of experiments $K_V \lesssim 0.1$). However, the technological reasons would hardly allow C_g/C to be more than about 5. Also, the gate capacitance increases the total capacitance of the central island, so too large C_g would substantially decrease the maximum operation temperature. As a result, the SET-based logic should operate at $K_V \sim 2$.

Let us first discuss the operation of the buffer/inverter as a simplest basic gate of the SET logic. The inverter can be easily realized by one SET-transistor in series with a load resistor R_L. Notice that the fabrication of such a resistor is not a big problem in contrast to the resistor for R-SET because there is no limitation on its stray capacitance. However, in the integrated circuits it would be more reasonable to use a tunnel junction instead of the load resistor [83]. The capacitance of this junction is not important because it is in parallel with the relatively large load capacitance C_L.

Figure 4 shows the control curves of the inverter with 'typically good' [35] parameters $C_g/C = 3$ and $R_L/R = 10$ (the symmetric transistor $C_1 = C_2 = C$, $R_1 = R_2 = R$ is obviously the best choice). One can see that the voltage gain decreases with temperature rather fast. When it becomes less than unity at $V_{out} = V_{in}$, the inverter cannot be used any more as a buffer restoring the binary voltage levels, so this condition determines the maximum operation temperature T_{max} of the buffer/inverter. (The same condition determines the presence of two stable states in the flip-flop made of two inverters connected in a circle.) For the parameters of figure 4,

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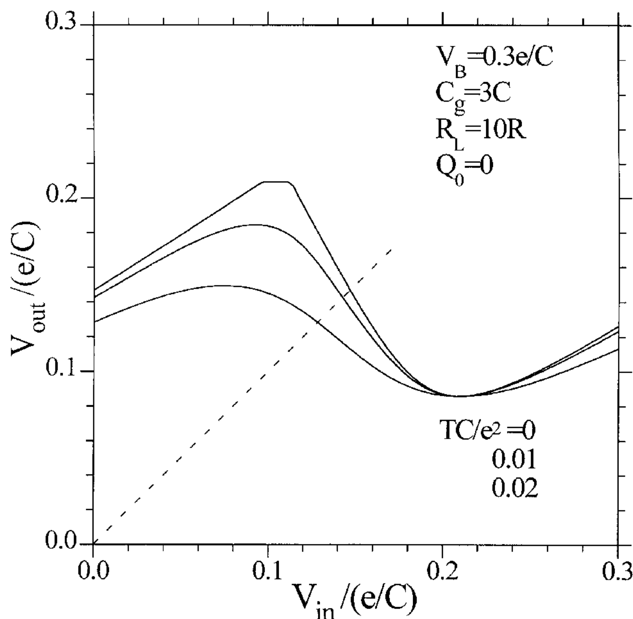

Figure 4. The control curves for the inverter based on resistively loaded SET-transistor for different temperatures.

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$T_{\max} \sim 0.015e^2/C$. The numerical search for the optimal parameter set in order to increase the operation temperature gives the result [35]

$$\left.\begin{array}{lll} T_{\max} \simeq 0.026e^2/C & \text{at } C_g/C \simeq 2, & Q_0 \simeq 0.1e \\ V_B/R_L \simeq 0.02e/RC, & R_L \gg R & \end{array}\right\} \qquad (6)$$

The maximum operation temperature significantly decreases when the ratio R_L/R becomes less than ~ 10. The necessity of relatively large R_L means that the additional power dissipation in the load resistor will be much larger than in the SET-transistor.

To reduce the power consumption the complementary circuits can be used [8, 34–36]. In contrast to CMOS technology in which n-MOS and p-MOS transistors are physically different, both complementary SET-transistors can be physically identical. To achieve the complementary action, the operating point of one transistor should be on the rising branch of $I - V_g$ dependence while for the other transistor it should be on the falling branch. This can be done with the use of additional capacitors [34] or different background charges Q_u and Q_d in complementary transistors [35] (figure 5). However, even without any special effort, complementary action occurs automatically in the simplest case of two symmetrical transistors with zero background charges [35]. (It is interesting that in terms of the maximum operation temperature this simplest case is very close to the optimal one.)

Figure 6 shows the control curves of the complementary inverter for different background charges at $T = 0$. An important feature of the complementary inverter is that both of the serially-connected SET-transistors may be 'closed', i.e. be in the Coulomb-blockade state. For example, curves 1 and 4 widen into 'uncertainty regions'. Inside these regions both transistors are closed and the current vanishes,

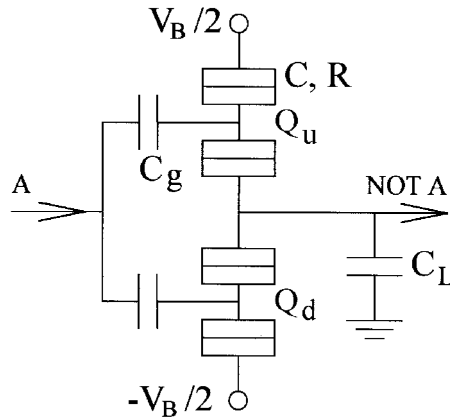

Figure 5. The complementary inverter made of two SET-transistors.

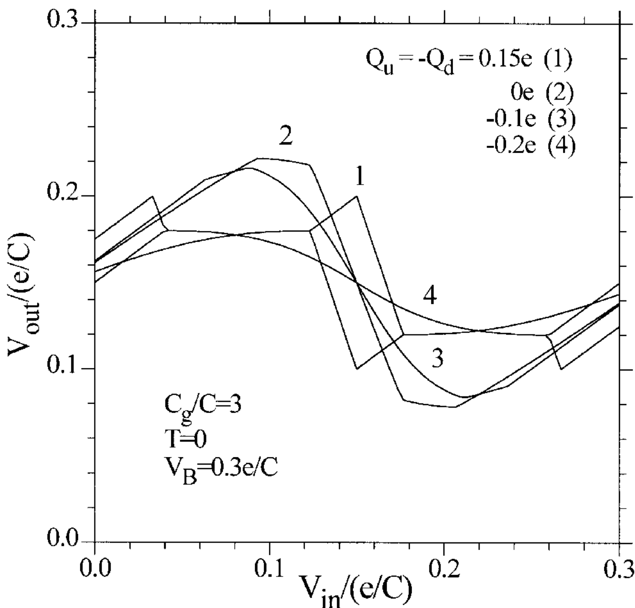

Figure 6. The control curves for the complementary inverter at $T = 0$ for different background charges of SET-transistors.

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so that the output voltage V_{out} is arbitrary within limits. The uncertainty regions become wider with a decrease of the dc bias voltage V_B.

For any finite temperature the boundaries of the Coulomb blockade are no more exact. Formally, in this case it is always possible to calculate the single-valued dependence of the output voltage corresponding to the exponentially small current I through transistors. This single-valued dependence can be calculated even at $T = 0$ if we take the cotunnelling [62] into account. However, it does not have much sense for the analysis of the parameter margins of the device (while it is meaningful for the calculation of static power dissipation). This is because if the currents are too small,

the time necessary for charging the load capacitance to reach the stationary state may be very long. So, the concept of the uncertainty regions can be still applied introducing some minimum recharging current corresponding to maximum acceptable recharging time [35]. At relatively high temperatures the leakage currents are sufficiently large and the uncertainty regions disappear.

Figure 7 shows the operation window of the symmetric complementary inverter with zero background charges (the criterion is the existence of two stable states in the line of inverters or in the flip-flop). The maximum temperature $T_{\max}$ (at which the window disappears) in this case is about $0.024e^2/C$. The numerical search for the maximum possible $T_{\max}$ in the space of all parameters gives the result

$$\left.\begin{array}{ll} T_{\max} \simeq 0.026e^2/C & C_g/C \simeq 2 \\ Q_u = -Q_d \simeq -0.1e, & V_B \simeq 0.27e/C \end{array}\right\} \quad (7)$$

Similar to the case of a resistively loaded inverter, the choice of symmetric SET-transistors ($C_1 = C_2 = C$, $R_1 = R_2 = R$) provides the maximum operation temperature if we assume that the minimum junction capacitance C is limited by the technology. (For example, the non-symmetric case considered in [34] corresponds to $T_{\max}$ as low as $0.0056e^2/C$.) Note that the maximum temperature, the corresponding gate capacitance and the background charge given by equation (7) exactly coincide with the result for a resistively loaded inverter with $R_L/R \to \infty$ [equation (6)] that can be easily understood from the symmetry arguments for the complementary inverter.

The optimal gate capacitance corresponds to the trade-off between too low voltage gain for small C_g and too large total island capacitance for large C_g. The

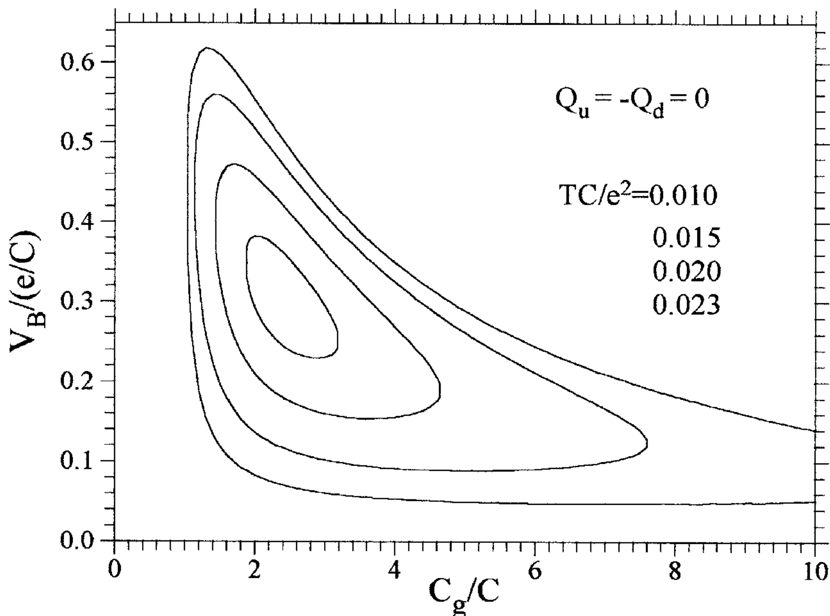

Figure 7. The parameter window for the operation of complementary inverter on the plane of the gate capacitance and bias voltage [35].

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maximum temperature is achieved at $C_g \simeq 2C$. However, at lower temperatures the total island capacitance becomes a less important factor, leading to the increase of the optimal C_g which corresponds to the largest parameter margins (see figure 7). As a result, $C_g/C \approx 3$ seems to be more or less the best choice for the experimental realization.

At $T \sim 0.01e^2/C$ the allowed fluctuations of gate capacitances and bias voltage are more than $\pm 50\%$ (figure 7). However, the margins for the fluctuations of background charges are not that wide, typically each background charge should be controlled with an accuracy of about $0.1e$.

The operation point which optimizes the maximum temperature of the complementary inverter corresponds to relatively large static power consumption about $2 \times 10^{-3} e^2/RC^2$ per SET-transistor. This magnitude is similar to that in the resistively-loaded case (if we neglect the dissipation in the load). On the other hand, in semiconductor electronics the complementary logic makes a considerable reduction in power consumption possible. Such a reduction is possible for the complementary single-electron inverter as well, but with the price of some reduction in operation temperature and parameter margins. The 'power saving' mode is realized when both transistors are well below the Coulomb blockade threshold (this also means that the recharging of the output line can be slow within 'uncertainty regions'); for the symmetric transistors this mode is achieved when the background charges are relatively far from zero. Figure 8 shows static power consumption per inverter for $Q_u = -Q_d = -0.2e$. Solid lines represent the results of the orthodox theory. It can be seen that at $T \lesssim 0.01e^2/C$ the power can be made less than $10^{-4} e^2/RC^2$ per inverter. The static power consumption is due to the leakage current in the Coulomb blockade state which can be caused not only by the finite temperature

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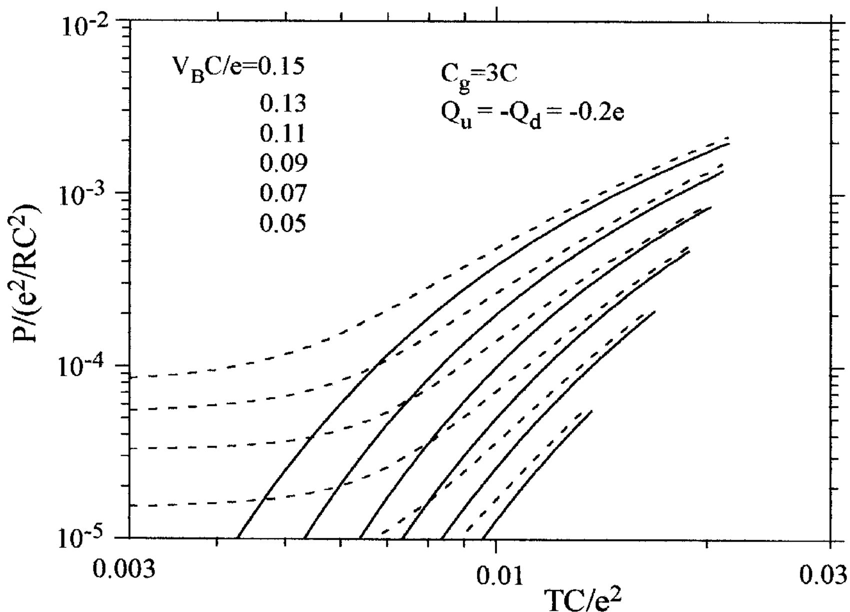

Figure 8. Power consumption P per complementary inverter in a 'power saving mode' as a function of temperature [35]. The solid lines represent the result of orthodox theory while for the dashed lines the cotunnelling is also taken into account ($R = 30R_Q$).

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but also by the cotunnelling processes [62]. The numerical results with the account of cotunnelling for $R = 30 R_Q \simeq 200$ kΩ are represented in figure 8 by dashed lines.

The switching time of the complementary inverter (defined as a switching time of the flip-flop made of two inverters) is close to $3RC_L$ [35]. One should reduce the load capacitance C_L (see figure 5) in order to increase the speed. However, if C_L becomes comparable to the junction capacitance C, then the fluctuations of the output voltage become comparable to the output signal, and the inverter cannot be considered as a reliable device. The reason is the shot noise of the current through SET-transistors [57]. Because the tunnelling is a random process, the number of electrons supplied to the load capacitance by one transistor is not exactly equal to the number of electrons drained through the other transistor, while each extra electron leads to the output voltage change of $\Delta V_{out} \simeq e/C_L$.

The relaxation to the equilibrium is due to the corresponding change of the currents through transistors, so the relaxation time is proportional to the effective differential resistance $R_d = R_{d1} R_{d2} / (R_{d1} + R_{d2})$ of two transistors which can be especially large when both of them are inside the Coulomb blockade range. For $C_L \gg C$ the rms fluctuation of the output voltage is given by $[(S_{I1} + S_{I2}) R_d / 4C_L]^{1/2}$ where the low frequency fluctuations of the currents through transistors can be estimated by Schottky value [57], $S_{I1} \sim S_{I2} \sim 2eI$. For the reliable operation C_L should not be less than $\sim 300C$ that corresponds to about 30 electrons on the load capacitance for the typical difference between two digital levels.

So far we have discussed the operation of the buffer/inverter made of SET-transistors. (Almost all results of analysis of the inverter are directly applicable to the two-inverter flip-flop which can be used as a SRAM-type memory cell.) The analysis of logic gates gives similar results while the operation temperature and parameter margins are somewhat lower. A possible structure of the NOR gate [36] is shown in figure 9(a). Notice that in contrast to the SET inverter which is similar to the circuit used in conventional digital electronics, design of the SET NOR gate differs from the conventional one. The direct reproduction of the design is impossible

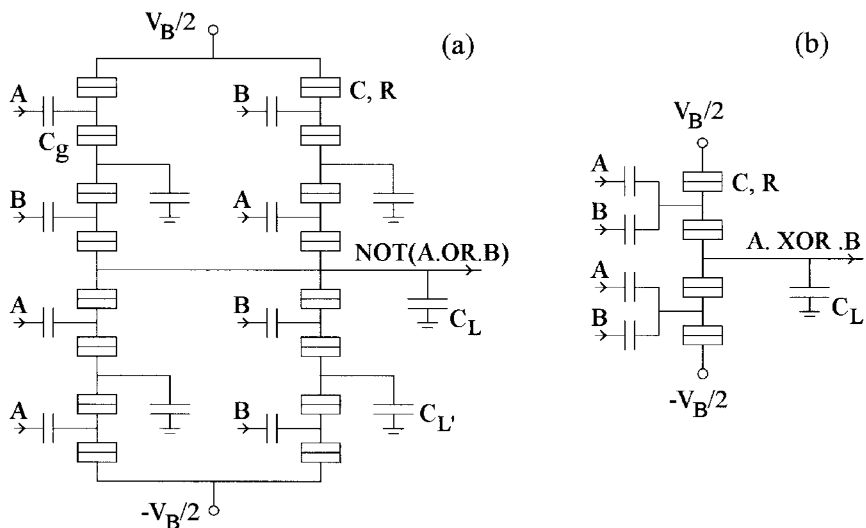

Figure 9. The possible design for the (a) NOR gate and (b) XOR gate of SET logic [36].

because of different characteristics of SET and MOSFET transistors. Due to the symmetry of the NOR gate and its nominal logic levels, inversion of the dc bias voltage transforms a NOR gate into a NAND gate with similar characteristics.

Numerical analysis [36] has proven that the inverter and both two-input gates can operate with the same bias voltage and use the same nominal logic levels (which are defined as stable voltage levels in a long line of inverters). The maximum operation temperature of this complete logic set is about $0.01e^2/C$. To have reasonable parameter margins, the temperature should be approximately half of the maximum temperature. For some specific parameter set analyzed in [36] it has been shown that at $T = 0.005e^2/C$ the NOR and NAND gates, and the inverter can sustain bias voltage fluctuations greater than $\pm 50\%$, variations in all coupling capacitances of $\pm 8\%$, and variations in all junction capacitances or tunnel conductances greater than $\pm 40\%$. The margin for the background charge variations is found to be about $0.03e$, the logic delay within the range $(2\text{–}20)RC_{\mathrm{L}}$, and the power consumption on the order of $3 \times 10^{-3} e^2/RC^2$ per transistor.

NOR and NAND gates accompanied by the NOT gate (inverter) are more than sufficient for performing arbitrary logic functions. However, the addition of other gates can help to make the logic more efficient. For example, figure 9(*b*) shows the possible design for the XOR gate [36]. The output voltage swing of this gate is somewhat lower than for NOR and NAND gates, but its performance can be easily improved by the addition of one or two buffer stages.

Let us now discuss the parameters and problems of the possible experimental realization of the logic based on SET-transistors. For a technology with a minimum feature size of 2 nm one can expect the capacitances of the tunnel junctions as low as 3×10^{-19} F. This corresponds to $e^2/C = 6 \times 10^3$ K; hence, the maximum temperature at which a SET-transistor still amplifies the voltage is close to 150 K. It would allow the reliable operation of the SET inverter at the liquid nitrogen temperature. However, for the logic gates this temperature is slightly above $T_{\max}$, and sufficient parameter margins are realized only at $T \sim 30$ K. Possibly the liquid nitrogen temperature can be achieved using recently analyzed multiple-junction SET-transistors [84] which promise about 2.5 times increase in the operation temperature in comparison with usual SET-transistors (the idea is to use the array of junctions and in this way reduce the total capacitance of conducting islands). In any case we see that the room temperature operation would require the fabrication technology at sub-1 nm level that could be accessible only for the molecular electronics.

For the estimate of the typical switching time let us take $R \approx 300\ \mathrm{k\Omega}$ and $C_{\mathrm{L}} \approx 10^3 C \approx 3 \times 10^{-16}$ F, then this time is about 1 ns. This value is not too spectacular but still acceptable even for future digital devices. The power consumption per transistor is quite small, about 3×10^{-9} W for the parameters above in a typical operation point. (In a 'power saving' operation mode it could be down to about 10^{-10} W, but this mode has not been studied for the logic gates so far.) However, at very large integration density the power dissipation becomes a very serious problem. For example, at 10^{11} transistors per cm^2 even in the power saving mode the total power is of the order of 10 W/cm^2 while in the typical mode it is over 100 W/cm^2.

Another principal problem of the logic based on SET-transistors is the necessity to keep fluctuations of background charge within the margins of the order of $0.03e$. This is a common problem for any integrated single-electronics, and the radical solution is known now only for the single-electron memory (which we will discuss in a separate section).

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Despite very serious problems at high integration level, let us emphasize that a logic device consisting of a small number of SET logic gates is relatively easy to fabricate using present-day technology. For the standard aluminium double-angle fabrication technique with $C \sim 10^{-16}$ F such a device will reliably operate at $T \sim 0.1$ K. The temperature could be possibly moved to ~ 10 K range using present-day high-temperature SET-transistors if the problems of large gate capacitance and interconnections could already be solved in these technologies.

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4. SEL logic

The presence of the static power dissipation due to leakage currents through SET-transistors and the necessity to move many electrons to/from the load capacitances in the SET-based logic, are the main reasons to look for another principle of operation of single-electron logic. The main idea is to represent the digital information not by voltage levels (as in the conventional and SET-based logic) but directly by single electrons on the conducting islands [37–48]. The circuits based on this truly single-electron approach are called single-electron logic (SEL) [37–39]. Besides the apparent advantage in the power consumption SEL-logic should also be considerably faster than SET-based logic because the processing of one bit of information requires only a few tunnelling events.

Figure 10(*a*) shows the basic cell of the SEL family proposed in [38–40]. Note that it is similar to the complementary SET inverter (figure 5). However, the important difference is that the capacitance of the middle island of a SEL cell is of the order of the junction capacitance (in contrast to large C_L in SET inverter). Inputs X and Y determine the charge state of the middle island. For example, if the lower branch of the cell is 'closed' by the signal Y, and the signal X opens the upper branch of the cell, then one extra electron tunnels through the upper branch to the middle island. This creates digital unity. Parameters are chosen in a way that the next electron cannot come because of the increased potential of the island. The extra electron can be removed (creating digital zero) from the middle island by closing the upper branch and opening the lower one. The charge of the middle electrode being the output of the cell, is used to affect the charge state of the next cell.

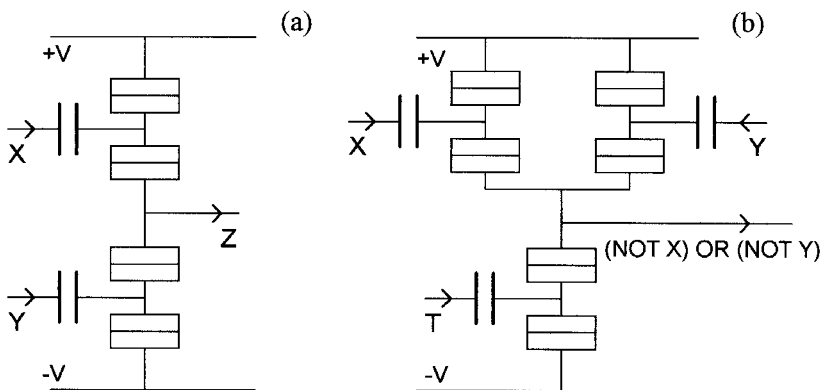

Figure 10. (*a*) The basic cell of the SEL logic and (*b*) the SEL NOR gate [38–40].

Figure 10(*b*) shows the SEL logic gate NOR. Signals X and Y are logic inputs. The middle island becomes charged by an extra electron when one of the upper branches opens. Clock signal T discharges the middle island at the end of the clock period (upper branches should be closed at this time).

In contrast to the SET-transistor circuits, there is a strong back action from the output to the input in SEL circuits. Numerical simulations have proved [38–40] that the proper choice of parameters provides the unidirectionality of the signal propagation. However, because of the back action, the parameter margins should be obviously considerably narrower than in SET-based logic.

Another problem of SEL logic is that the information coded by only one electron can be destroyed by a single erroneous event due to cotunnelling or thermoactivated tunnelling (in contrast to SET-based logic in which these processes are allowed and do not affect the digital information). The possible solution would be the use of multi-junction arrays as branches of SEL circuits to reduce the probability of erroneous events. However, this possibility has not yet been studied quantitatively.

The fragility of the information coded by single electrons and narrow parameter margins make SEL logic circuits much more difficult to implement than SET-transistor logic, at least at the present stage. However, simple SEL-type circuits based on the single-electron parametron (considered in §6) can be demonstrated using present-day technology.

In the next two sections we consider two specific types of SEL logic in more detail.

5. Wireless single-electron logic

In both SET-transistor circuits and SEL logic considered above, the interconnections between the circuit elements as well as the power supply require the use of wires. Though the necessity of wires is not a principal problem, it is obviously inconvenient at the few-nanometre size scale. In the wireless single electron logic proposed in [43] the power is supplied by an alternating external electric field, and the capacitive coupling between neighbouring cells is due to their close location.

The 'device' consists of many conducting islands, and the logic functions are determined by their specific arrangement (figure 11). Small 'puddles' of 2D electron gas, small metallic droplets on an insulating substrate, or conducting clusters in a dielectric matrix are possible implementations of the islands. The basic cell of the logic is a short chain of closely located islands so that electrons can tunnel between neighbouring islands. There is no tunnelling between different chains because of the larger separation.

Application of in-plane electric field E creates the voltage between the islands. When E exceeds the Coulomb blockade threshold E_t, the tunnelling occurs somewhere inside the chain, producing an electron–hole pair. The electric field drags the components of the pair apart towards the opposite edges of the chain, creating the polarized state. If now the field E is decreased, the pair eventually annihilate. However, it will occur at the field E_a considerably smaller than E_t. Stability of both polarized and non-polarized states for E between E_a, and E_t allows one to use these states as logic unity and zero.

The polarization change can propagate along a line of closely located chains [figure 11(*a*)]. Suppose that all chains are not polarized initially, and E is slightly less than E_t. This is a metastable state. If one chain becomes polarized, the field of

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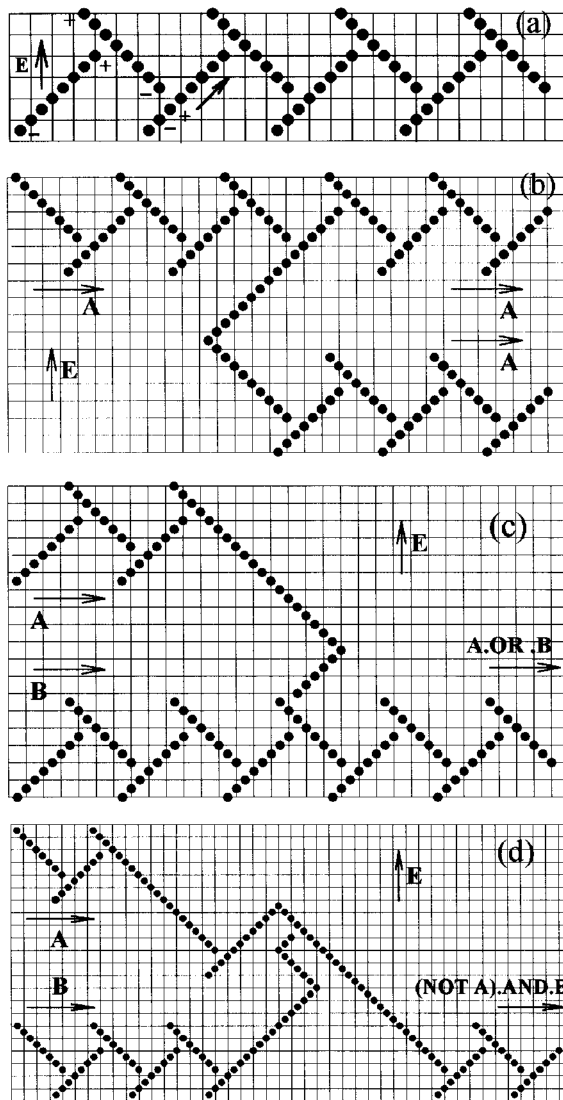

Figure 11. Wireless single-electron logic [43] based on tunnelling between small conducting islands and biased by electric field E. (a) The propagation line, (b) the circuit for the signal fan-out-two, (c) the logic gate OR (gate AND has a similar design), and (d) the gate (NOT A).AND.B which can be used as an inverter. The square lattice is a guide for eyes.

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extra electron (hole) on the edge island increases the potential difference between neighbouring islands of the next chain [figure 11(a)]. This makes tunnelling energetically favourable and leads to polarization of the next chain. This in turn polarizes the next chain and so on.

The line of chains shown in figure 11(a) allows propagation perpendicular to external field from left to right. The unidirectional propagation is a consequence of the asymmetry of the circuit; a mirror image of this line would allow propagation from right to left. Propagation with a velocity component along the field or opposite

to it can be achieved even more easily by the use of one long chain. The natural fan-out of the signal into two lines can be realized if both edge islands of a chain are used to trigger the next chains [figure 11(*b*)].

A 'bi-controlled' chain [fifth from the right in figure 11(*c*)] which can be triggered by the polarization of either of two neighbouring input chains can be used as the basic part of the logic gate OR. The logic gate AND can be designed similar to the OR gate, but with slightly larger distance between the 'bi-controlled' chain and the neighbouring input chains, in order to decrease their influence. Another possibility is to make the islands of 'bi-controlled' chain slightly smaller in order to increase the Coulomb blockade threshold.

Because of the asymmetry between logic unity and zero the design of the inverter is relatively complex. The circuit shown in figure 11(*d*) implements the logic function (NOT A).AND.B if the signal from input A comes before the signal from input B. The signal B will propagate to the output as in the usual propagation line, unless the chains of input A are polarized. This circuit can be used as NOT A, if logic unity always comes from input B and it comes later than signal A. The relative delays of signals can be adjusted using propagation lines of the proper length or controlling the tunnel resistance.

According to numerical simulations (based on orthodox theory), the correct operation of the circuits shown in figure 11 requires that the magnitude of external field E lies within $\sim 5\%$ margin [43] (the propagation line being the simplest circuit allows a somewhat wider margin $\sim 9\%$). This number also gives a crude estimate of the margins for other parameters (fluctuations of radius, spacing, etc.).

The logic gates considered, together with propagation lines and fan-out circuits, are sufficient for computing. In the simplest mode of operation, all chains inside a device initially have zero polarization and external field is zero. Then external field increases up to a value for which all gates operate correctly, and cells start to switch in accordance with the input information flowing from the edges of the device. The result of the computation is the final polarization of output cells which can be read out, for example, by single-electron transistors. This simplest mode of operation can obviously be improved by the use of periodic changes of the external field ('clock cycles'). Properly chosen levels of the field can reset some cells but preserve the information in other cells. Performance can be improved by the use of elements with different Coulomb blockade thresholds and use of two in-plane components of external field.

There is no static power consumption in the wireless single electron logic, and the energy is dissipated only during information processing. The estimate for the metallic islands with 2 nm radius gives a quite small value of 3×10^{-20} J per island per switching. However, at very large integration scale even this value can lead to unacceptable power consumption. For example, for the density 10^{12} islands/cm^2 and the clock frequency 10^9 Hz one finds a power about 30 W/cm^2. The use of non-zero background charges can reduce the necessary external field and, hence, the power consumption.

Let us mention that the wireless single electron logic proposed in [43] somewhat resembles the earlier proposed ground state computing devices [46, 48]. In both ideas there are no wires, the information is coded by the bistable polarization of the basic cell and the 'geometrical' coupling of nearest neighbours due to their close location is used. The main difference is the absence of any external biasing in ground state computing, so that the only driving force is the fixed polarization of the cells at

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the 'edges' of the device. If such a device is required to operate in a mode of sequential switching of cells, then the small total energy gain (proportional to the number of 'edge' cells) should be distributed evenly between all 'bulk' cells. Hence, the parameter margins would be roughly inversely proportional to the size of the device, and only small devices could operate in a classical sequential mode [48] making reasonable integration impossible for ground state computing. While the sequential switching of cells is not possible, the system as a whole should eventually reach the ground state. However, then a significant part of the device should be involved in the macroscopic quantum process ('simultaneous' switching of many cells), so this transition would require practically infinite time because of the exponential dependence on the number of cells.

In contrast to the ground state computing, the wireless single electron logic uses external biasing that allows the traditional computing by the sequential switching of cells in the device of arbitrary large integration scale. Notice that recently there was a considerable development [47] of the initial idea of the ground state computing. Using the external control of the cells by the alternating gate voltage and applying the principle of operation similar to that of single-electron parametron, it becomes possible to provide sequential switching of cells in the integrated circuit.

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6. Single-electron parametron

In a SEL-type logic the switching of a cell typically requires the energy on the order of only e^2/C where C is the typical capacitance. However, this dissipation can be further reduced. In the logic based on the single-electron parametron [44, 45] (also called SET parametron) the dissipation can be even lower than the 'thermodynamic limit' of $T \ln 2$ per bit for the reversible logic gates. We will consider the wireless implementation of SET parametron biased by the rotating electric field. However, the implementation suitable for the standard present-day technology is also possible.

The basic cell of the SET parametron consists of three conducting islands [figure 12(*a*)]. The middle island is slightly shifted off the line passing through the centres of the edge islands. Electrons can tunnel through small gaps between the middle and edge islands, but not directly between the edge islands because of their much larger spacing [figure 12(*a*)].

Let us assume that the cell as a whole is charged by one uncompensated electron (this makes the explanation of the operation principle simpler; later we will consider a more natural case of an initially neutral cell). If the cell is biased by the sufficiently strong 'clock' electric field E_c opposite the y axis [see figure 12(*a*)], the electron is obviously located at the central island. Now let the field be decreased gradually so that eventually it changes direction for positive (along the y axis). At some moment the electron will have to tunnel to one of the edge islands because these states become energetically preferable. Because of the geometrical symmetry, the choice of the island (left or right) will be random, i.e. the charge symmetry will be broken spontaneously.

However, if there is a weak 'signal' field E_s along the x-direction (which may be applied, for example, by the neighbouring similar cell), the final position of the electron will depend on the sign of E_s. A natural way to discuss this effect is to say that the signal field E_s creates an energy difference Δ between the electron states in islands 1 and 3, and that the electron prefers to tunnel into the island with the lowest energy state [figure 12(*b*)]. If now the clock field E_c becomes large, it creates a

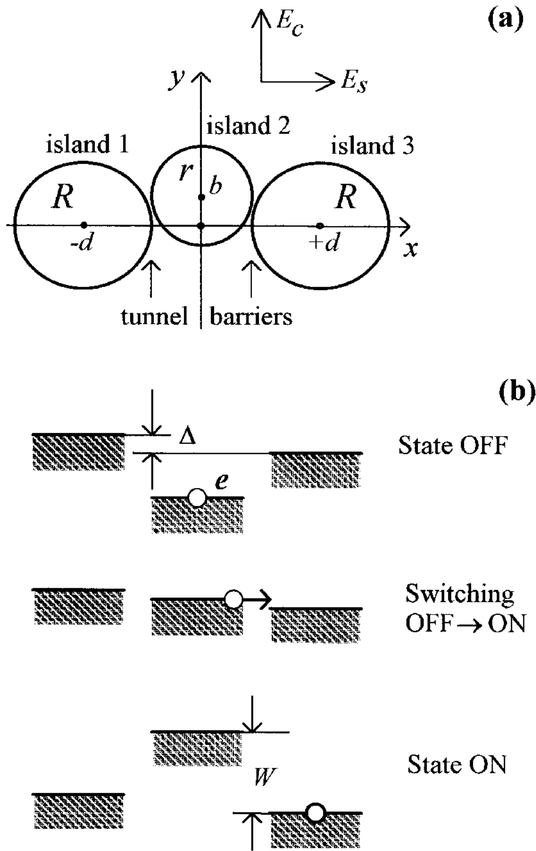

Figure 12. (*a*) the basic cell of the SET parametron consisting of three conducting islands [44]. Electrons can tunnel between the middle and edge islands. (*b*) Energy diagram of the cell charged by one extra electron for three values of the bias field E_c.

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high energy barrier W [see figure 12(*b*)] between the edge islands, so that the electron is reliably trapped in the island it has tunnelled to, regardless of the further changes of the signal field E_s.

Thus if fluctuations in the system are low enough, and the clock field changes slowly enough, even a small field E_s of the proper sign at the decision-making moment (when $W(t) = 0$) is sufficient to ensure a certain robust final polarization of the cell. This process can be interpreted as a reliable recording of one bit of information (for example, the electron on the right island can mean digital unity while the electron on the left island encode digital zero). Now the dipole moment of the cell in turn can be used to produce the signal field to control the other cells during their decision-making moments, and hence determine their information contents. (The operation principle of SET parametron is similar to that of the Josephson junction device called parametric quantron [85]. The important difference is the discrete internal degree of freedom of SET parametron in contrast to the continuous Josephson phase in parametric quantron.)

If the SET parametron cell is initially neutral (that is a more natural assumption), then the application of the sufficiently large clock field E_c in either positive or

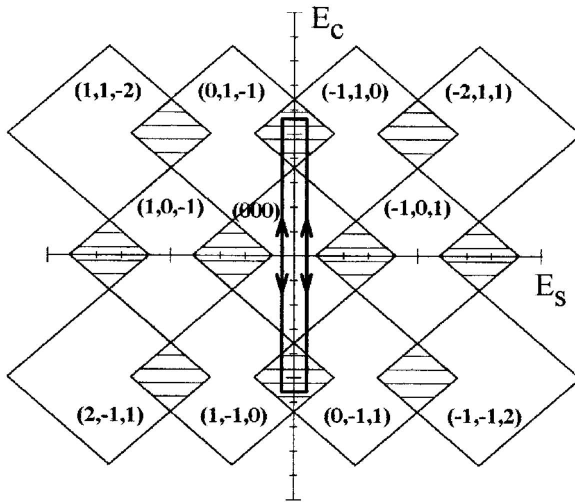

Figure 13. The diagram of the stable charge states of a typical initially uncharged SET parametron cell. Bistable regions (which correspond to ON states) are shaded. Thick line illustrates the periodic operation of the cell.

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negative direction creates the electron–hole pair. Similar to the case considered above, there is a bistability for the sign of the dipole moment, and the final state is determined by the sign of the signal field E_s.

Figure 13 shows the phase diagram of an initially neutral cell with some particular geometry ($R/r = 1$, $d/r = 3$, $b/r = 1$, $q_{i0} = 0$). The regions of bistability where either of two charge states is locally stable are shaded. They correspond to ON states of the SET parametron while the remaining (monostable) part of the phase diagram corresponds to OFF states of the system. If the signal field E_s is low (as we suppose), only the set of diamonds along the axis E_c is implemented. The arrowed rectangle illustrates the periodic switching of the cell caused by periodic clock field E_c (two OFF → ON and two ON → OFF switchings per period of E_c). One can see that the sign of a small E_s field determines which diamond boundary will be crossed first and hence determines the charge state of the system within this bistable region.

Figure 14 shows an implementation of shift register using SET parametron cells [44]. The direction of the middle island shift is turned by $\pi/3$ (in y–z plane) each next cell. The system is driven by the clock field rotating in the same plane. This rotation provides the shift of E_c (which is now the component of the clock field in the plane of the corresponding cell) by 1/6 of the clock period for each next cell. When a cell is in the ON state, its dipole electric moment creates the signal field E_s which is especially strong for its nearest neighbours, and thus determines the direction of electron tunnelling when the next neighbouring cell is turned ON. Notice that when a cell is switched from OFF to ON, one of the neighbours is in an ON state while the other neighbour is in a symmetric OFF state and does not influence the decision. The polarizations of other cells create some uncontrolled contribution to the signal field E_s. However, its magnitude is much smaller than the field from the driving nearest neighbour, and the tunnelling direction is unambiguous. For the circuit shown in figure 14 the signal propagation is six steps per period of field rotation, and the transmission rate is two bits per period, so on average each bit requires three cells.

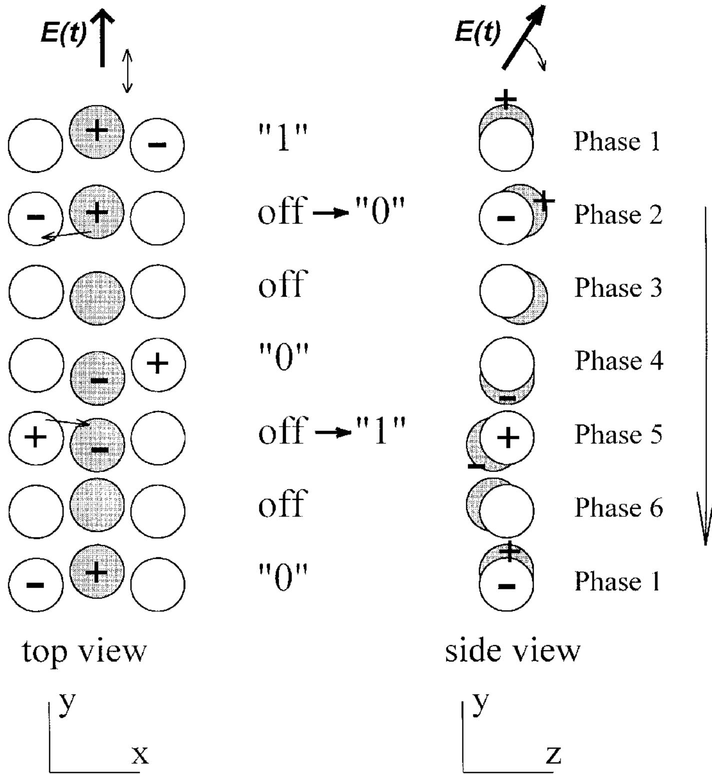

Figure 14. The top (left) and side (right) views of a shift register based on the SET parametron [44]. The clock field $E(t)$ rotates in the y-z plane. Digital bits are coded by the direction of the cell polarization and are propagated from the top of the figure to the bottom, over six cells during one clock period.

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The numerical simulations of the shift register have shown that to provide the broader margins, the elliptic polarization of the clock field rather than circular one should be used. More exactly, the out-of plane component A_z should be larger than the in-plane component A_y, because of the field screening in the z direction due to the finite size of the conducting islands. For some particular geometry considered in [45] the optimal ratio A_z/A_y has been found to be about 1.5, providing the margins for the clock field amplitude as wide as $\pm 30\%$. The margins are considerably narrower for parameters which destroy the geometric symmetry of the parametron cells. For example, the allowed fluctuation of the x-axis of a cell is only about $\pm 0.4°$ (this value could be improved using another geometry).

The shift register shown in figure 14 is actually a line of inverters. To have a complete set for the arbitrary logic functions we need to have other logic gates (e.g. NAND or NOR), and a circuit with a fan-out more than one ('splitter'). All these functions can be naturally implemented using the geometry shown in figure 15. If the clock field rotation causes the signal propagation from the bottom to the top we get a fan-out-two circuit, because the dipole moment of cell F (in its ON state) will determine the charge state of both cell A and cell B during their OFF → ON switching. On the other hand, if the signal propagates from the top to bottom, we get the implementation of a binary logic function (either $F = A.\mathrm{NOR}.B$ or

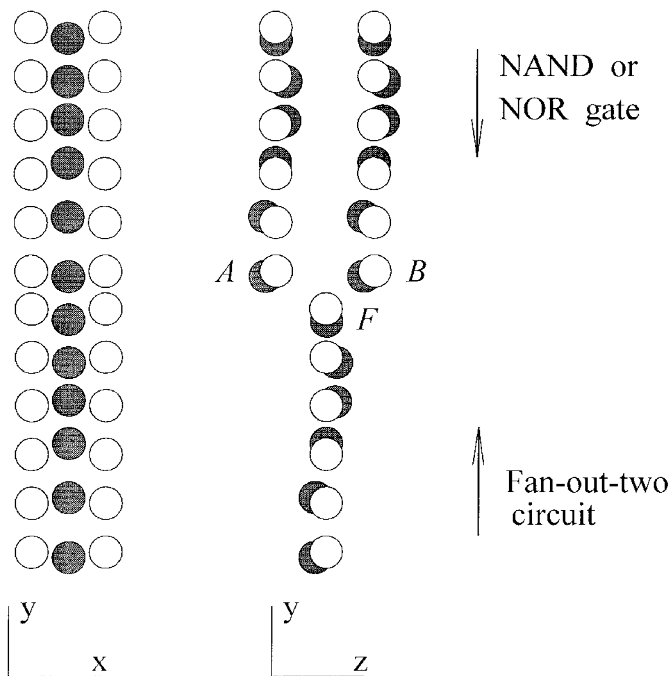

Figure 15. The circuit which can be used for the fan-out-two of a signal (if the propagation direction is from the bottom to the top), and also as a logical gate NAND or the gate NOR (for opposite signal propagation direction). The asymmetry required for NAND and NOR gates can be created by the background charges on the edge islands of cell F or by application of local electrostatic field.

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$F = A$.NAND.B, depending on the asymmetry provided by the background charges or local dc bias field imposed on cell F).

The numerical simulations [45] have proved the correct operation of the logic gates and the 'splitter'. The quasi-random bit sequences were used as digital inputs and the input/output lines were taken sufficiently long to check the influence of non-nearest-neighbour cells. The typical margin for the clock field amplitude was found to be about $\pm 10\%$.

One of the most important advantages of the SET parametron is the extremely low energy dissipation at sufficiently slow switching speed $\alpha = \mathrm{d}W/\mathrm{d}t$. Figure 16 shows the average energy dissipation ε per switching of a cell to ON (solid line) as a function of the dimensionless switching speed $\beta = (\mathrm{d}W/\mathrm{d}t)e^2R/T^2$ (here R is the tunnelling resistance) calculated using the orthodox theory [44]. The expression for the low-speed limit $(\beta \ll 1)$ can be obtained analytically by

$$\varepsilon = \kappa\beta T = \kappa\alpha e^2 R/T, \qquad \kappa \simeq 0.426 \tag{8}$$

which is represented by the dotted line in figure 16. In this quasi-reversible regime $\varepsilon \ll T$. It is curious that the energy dissipation decreases when the temperature increases.

In the opposite limit $(\beta \gg 1)$ the average energy dissipation is given by

$$\varepsilon = (\pi\beta/2)^{1/2}T = (\pi e^2\alpha R/2)^{1/2} \tag{9}$$

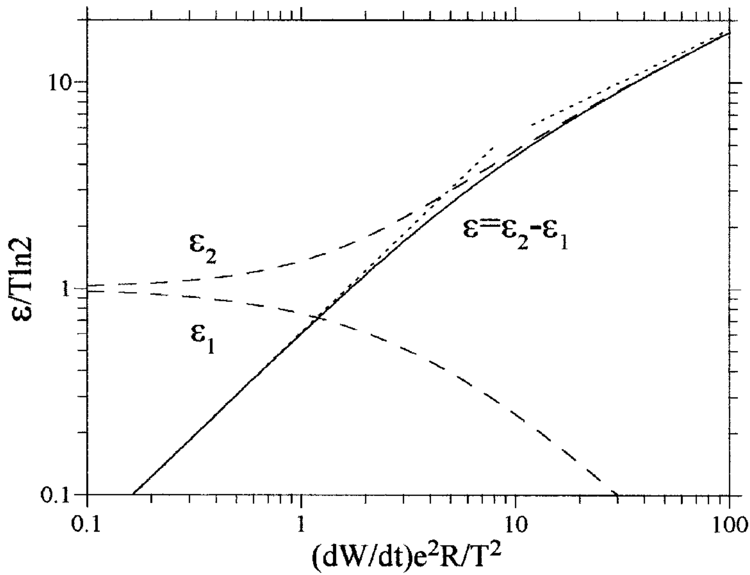

Figure 16. Solid line: the average energy dissipation during switching of a SET parametron cell as a function of the dimensionless switching speed $\beta = (\mathrm{d}W/\mathrm{d}t)e^2R/T^2$ [44]. Dashed lines: average cooling of the heat bath ε_1 during the first part of the process ($W \leq 0$) and its average heating ε_2 during the second part ($W \geq 0$). Dotted lines show the low-speed [equation (8)] and high-speed [equation (9)] asymptotes.

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(the other dotted line in figure 16), and it is much larger than the thermal energy, indicating the thermodynamic irreversibility of the switching process.

It is interesting to study the time dynamics of the heat transfer between the system and the environment ('heat bath') during the switching process. During the 'first part' of the switching process [when $W(t) < 0$] the electron tunnelling is possible only if it receives the energy from the heat bath, which, hence, is *cooled* on average. The lower dashed curve in figure 16 shows the average energy ε_1 borrowed from the heat bath during the first part of switching. During the second part $[W(t) > 0]$ the average energy $\varepsilon_2 > \varepsilon_1$ (the upper dashed line) is returned back to the heat bath leading to positive total dissipation $\varepsilon = \varepsilon_2 - \varepsilon_1$. Notice that in the adiabatic limit $\varepsilon_1 = \varepsilon_2 = T\ln 2$. This result is due to the relation $\varepsilon(t) = -T\Delta S_{\mathrm{inf}}(t)$ between the energy and the entropy $S_{\mathrm{inf}} = -\sum p_i \ln p_i$ of the degree of freedom used to code information [86, 87] (p_i are the probabilities of different charge states). In fact, in the instant when $W = 0$, the system may be in either of two states with equal probabilities $p_1 = p_2 = 1/2$, hence $\Delta S_{\mathrm{inf}} = \ln 2$ has been acquired in comparison with the definite initial state ($p_1 = 1$, $p_2 = 0$). By the end of the switching the informational entropy is restored to the initial value since the state is definite again ($p_1 = 0$, $p_2 = 1$).

The general thermodynamic arguments lead to the conclusion that erasure of information necessarily requires the energy dissipation of at least $T\ln 2$ per erased bit [86, 87]. During the switching OFF → ON of a cell in any SET parametron circuit, the amount of information is not changed, allowing arbitrary small energy dissipation in the low-speed limit. However, for switching ON → OFF the lower bound is determined by logical reversibility.

The SET parametron shift register is obviously a logically reversible circuit because during cell switching to OFF the information is preserved by the next cell. One can check that the sign of the energy difference Δ between two digital states [figure 12(*b*)] does not change during ON phase because of the back influence from the next cell. So the cell stays in the lower-energy state and the analysis of the energy dissipation during switching to OFF is equivalent to that of the switching to ON. A similar small-dissipation case is realized in SET parametron fan-out circuit (figure 15), because during ON $\rightarrow$ OFF switching of the last cell of the input line (cell F in the figure) the proper sign of Δ is maintained by both first cells of the output lines.

The situation should be different for the NAND/NOR gate because any gate consisting of two inputs and one output is logically irreversible and, hence, has the lower bound [86,87] for dissipation of $T \ln 2$ per bit (on average, for input streams with equal probabilities of digital unity and zero). Actually, in the SET parametron realization shown in figure 15 the average energy dissipation is even much larger. If the input bits are different, then the energy difference Δ changes its sign during ON state of either cell A or B. Hence, during switching to OFF the energy dissipation is of the order of Δ which is much larger than T because $\Delta \gg T$ is necessary to ensure small error probability.

To realize the reversible NOR and NAND gates using SET parametron cells, one can use the gates with two inputs and three outputs (similar to the suggestion for the parametric quantron logic gates [85]). The input information is copied to the first cells of two additional shift register lines. If their coupling to the last cells of input lines is stronger than input–output coupling, then the proper sign of Δ is always maintained, and the energy dissipation is arbitrarily small in the slow switching limit.

The orthodox theory describes two types of possible digital errors in SET parametron circuits [44]. If the switching speed it too high, then the system can remain in the initial (symmetric) state up to the moment when the tunnelling to the wrong island becomes possible [see figure 12(*b*)]. The probability of the corresponding 'dynamic' error is given by the expression

$$P = \gamma \exp(-1/2\gamma), \qquad \gamma = (\mathrm{d}W/\mathrm{d}t) e^2 R/\Delta^2 \tag{10}$$

for $\gamma \ll 1$. At sufficiently low switching speed the dynamic error is exponentially small and the contribution from the 'thermal' error which occurs with the probability

$$P = \exp(-\Delta / T) \tag{11}$$

becomes important. Because of the exponential dependence, this probability can be also made negligible using sufficiently low temperature.

Besides these two kinds of errors, the wrong switching can occur due to the processes of cotunnelling. For illustration, the lowest energy diagram in figure 12(*b*) shows the situation when the charge state with higher energy is occupied, and the digital information in the cell is preserved by the energy barrier (higher energy of the symmetric state). According to the orthodox theory, the single-electron tunnelling in this case is impossible at sufficiently small temperature. However, the second-order cotunnelling, i.e. simultaneous tunnelling of two electrons through both junctions brings the system into the lower energy state and, hence, is energetically allowed. This process changes the sign of the cell dipole moment and can lead to the digital error.

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This type of error can occur, for example, in the considered shift register during the phase when the bit is stored by only one cell, and the long-range interaction with cells caring other bits (nearest cells are OFF) can provide uncontrolled sign of the energy difference Δ between digital states. The erroneous bit will then propagate along the shift register.

Cotunnelling is a common problem of any kind of SEL logic. Several means are available to reduce the cotunnelling error probability. First, because the rate of m-electron cotunnelling scales as $(R_Q/R)^m$ [62] while the single-electron rate is inversely proportional to the first power of the tunnel resistance R, the increase of R will decrease the relative importance of the cotunnelling processes. Another, more powerful method is to increase the smallest order m of possible cotunnelling processes. This can be done, for example, by increasing the number of cells which store the same bit. In the realization of shift register shown in figure 14 this goal is easily achieved by a decrease of the angle between the planes of neighbouring cells. If the bit is stored by k neighbouring cells then the error can occur only if all these k cells simultaneously change their polarizations and if the final state has a lower energy. So, the lowest order of erroneous cotunnelling is $2k$, and the linear increase in 'hardware' would allow the exponential reduction of the error probability. This idea solves the problem of cotunnelling not only for the shift register, but also for the logic gates.

The estimates show that for the realization of SET parametron logic using the conducting clusters with diameter of 5 nm, the maximum operation temperature (corresponding to the thermal digital error probability less than 10^{-10} per switching) is about 15 K. Assuming the same value for the dynamic error, we obtain the maximum clock frequency about 10^9 Hz for $R \sim 10^5\,\Omega$. In this case the power dissipation is as small as 10^{-11} W per cell. To achieve the quasi-reversible mode of operation the frequency should be lower than 18^8 Hz for this set of parameters at $T = 15$ K. For example, at $\upsilon \sim 10^6$ Hz the power dissipation is only about 5×10^{-18} W per cell. This figure makes possible even the three-dimensional integration. Although the clock frequency in this regime is clearly not spectacular, the computing power of the device can be very large if the 3D threshold can be overcome.

Notice that the operation of the SET parametron circuits requires the well defined background charges. The allowed fluctuations are of the order of $0.01e$. This is a common problem for any kind of single-electron logic (with the exception of resistively-coupled devices). However, if we imagine the potential molecular electronics technology for the SET parametron devices when the cells are reproducible on the molecular level, then the requirement of well defined background charges seems to be achievable in principle.

Simple SET parametron circuits, for example, the few-step shift register, can be realized using the present-day 'low temperature' aluminium technology. Instead of the rotating electric field, the biasing of three-island cells should be done in this case by additional gates which can also be used to adjust the background charges. The sequential application of the voltages to the row of gates in a 'running wave' mode would cause the propagation of information. The SET-transistor can be used for the readout. For the present-day technology the operation temperature of SET parametron circuits should be in sub-Kelvin range. Nevertheless, such an experiment would be quite interesting as the first demonstration of the logic with the information represented by single electrons.

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7. Logic or memory?

Besides the possible application in logic devices, the single-electronics could also be used in future ultradense memory circuits. The estimates and problems discussed in the previous sections show that the creation of single-electron logic is an extremely difficult problem, if it is possible at all. One can wonder if the problems are not so severe for single-electron memory. Generally this is true, and this makes the studies of single-electron memory much more important for future digital devices.

The basic reason why the single-electron memory is much easier to implement than the single-electron logic is that the logic device is necessarily a complex system consisting of many gates interacting in a specific way, while memory cells are independent, each of them being a simple circuit. The operation of logic circuitry requires something like voltage amplification to pass the information from gate to gate. In contrast, in the memory the storage of information can be done in a passive way, and for the readout only some sensing of the storage contents is sufficient (the amplification can be done at the next stage).

As an example, the SET-transistor can amplify the voltage only at $T < 0.026e^2/C$ where C is the junction capacitance [see equation (6) and (7)], while in the sensing mode it can be used at temperatures up to $\sim 0.13e^2/C$ (the modulation amplitude is still more than 10% at this temperature). The possibility to use five times higher temperatures is extremely important for single-electronics (actually this factor is even larger if the necessary parameter margins are taken into account). Moreover, in the sensing mode the problem of background charge fluctuations can be avoided (see next section) which is also extremely important for integrated circuits.

The operation of a memory cell basically consists of two stages: the storage of digital information and its readout. Here we do not consider SRAM-like memories which are similar to simple logic circuits but concentrate on DRAM and non-volatile memories. So, the digital bits are assumed to be represented by electric charges. Single-electron effects can be used in both information storage and readout (sensing).

The readout can be naturally done by SET-transistor. As we discussed above, the simplicity of the circuit (just one transistor is sufficient) and relatively soft temperature requirements make it suitable for integrated room temperature devices. Notice, however, recent experiments [31, 32] which showed that FET-like devices could probably still be used as sensors at least down to the 10-nm size scale.

For information storage the single-electron effects can be important in two different issues. First, the bistability of the memory cell can be provided by the Coulomb blockade so that there is no charge leakage for both states representing digital unity and zero. For example, the Coulomb blockade in the few-junction array has been used in experiments with so-called single-electron trap [24–26] (see also [27, 28]). The important problem which can make the retention time unacceptably small is the leakage due to thermoactivated processes or cotunelling. Another problem is the fluctuation of the Coulomb blockade threshold for random background in the array [51] (the usual addressing of a memory cell by word and bit lines requires the margin for the threshold voltage to be at least not larger than $\pm 30\%$, and this condition is rather strict for the array with random background charges).

As an alternative, even in the single-electron memory circuits the classical Fowler–Nordheim tunnelling can still be used (similar to flash memories [88]) to provide the threshold-like dependence of the storage island charging rate on the applied voltage, thus blocking the leakage of the stored charge and ensuring the bistability. This is because the physics of Fowler–Nordheim tunnelling does not lead

to principal difficulties when the typical device size is scaled down to few-nm range (in contrast, e.g. to the use of FET). This idea has been suggested for single-electron memory in [51] and also has been used in recent experiments [31–33]. Notice that the discreteness of the charge on the storage island can provide much sharper threshold of Fowler–Nordheim tunnelling, thus reducing the writing time.

The second issue in the charge storage, related to the single-electron effects is the number of stored electrons. At present in conventional electronics this number is about 10^4. The reduction of this number is very important for the power consumption and speed. So, when we speak about the single-electron memory, it is obviously assumed that not more than a few electrons should be stored. There is already a considerable number of experiments in which the controllable trapping of single electrons in different structures have been demonstrated [24–32]. In these experiments the digital bit can be represented just by one electron on an island similar to the idea, used in SEL logic. This is undoubtedly a very important experimental achievement. However, the question as to how many electrons should be stored in a practical single-electron memory cell is not so simple and deserves special discussion.

7.1. *One-electron and few-electron memories*

The memory cells with the one-electron representation of digital bits are very attractive and reach the principal limit in a sense that the number of stored electrons cannot be further reduced. However, in the author's opinion, the memory cells suitable for practical applications should necessarily operate with few (more than one) electrons. The reason is that for one stored electron, only one erroneous event is sufficient to destroy the whole information. Hence, for DRAM the information *refreshing* will be impossible, and for the non-volatile memory the reliability will also be quite poor. For example, even if the average retention time of a single electron as long as 10^{15} s can be achieved, the reliability of the whole device containing $\sim 10^{12}$ memory cells will be unacceptable.

To increase reliability it is possible to use the standard methods of the information redundancy. For example, each bit can be stored by three cells. However, it is obviously much simpler to use three electrons in each cell, so that the leakage of one electron still does not destroy the stored information. The linear increase of the number of stored electrons exponentially increases the retention time of a cell.

In the author's opinion, the optimal number of stored electrons per cell should be between five and 20. The further increase of this number would not only increase the power dissipation too much but would also lead to difficulties with the precise control of the number of stored electrons.

Let us emphasize that in contrast to conventional DRAMs, the number of stored electrons in few-electron memory cells should be controlled precisely (fluctuations are due to leakage only), so in this sense they can still be called single-electron memory cells.

8. Background-charge-insensitive single-electron memory

In this section we will discuss the idea of a few-electron memory cell with the readout by SET-transistor which can operate in the environment of random background charges, as proposed in [51].

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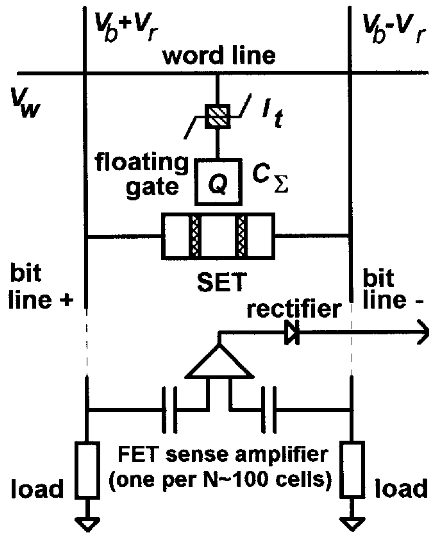

Figure 17. The schematic of the proposed ultradense hybrid SET/FET memory operating in background-charge-insensitive mode [51]. The information is stored as a few-electron charge Q of the floating gate.

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The random background charge Q_0 unpredictably shifts the periodic control curve of the capacitively coupled SET-transistor (figure 2). The basic idea of Q_0-insensitive operation of the transistor is to use it in a mode when the ramping input signal drives the SET-transistor through several periods of its control characteristic. In this case the output signal will oscillate, and for any initial Q_0 the amplitude of oscillation is equal to the maximal swing of the control characteristic. In the proposed memory cell (figure 17) this signal is further amplified by FET sense amplifier and after rectification serves as the final output. In order to prevent the contamination of the SET signal by the Q_0-dependent dc background, a high-pass filter (for example, the blocking capacitor) may be used between the SET and FET stages. The use of FET solves the problem of relatively high output impedance of a single-electron transistor which in this case should charge only a sufficiently small load capacitance of a short interconnecting line.

As in traditional non-volatile semiconductor memories [88] digital bits are stored in the form of electric charge Q of a floating gate located in the vicinity of the SET-transistor. In the case of a very small gate (of the order of 10 nm) this charge is just a few (10–20) electrons. The charge can be changed, for example, by its injection/extraction through the relatively thick dielectric layer via Fowler–Nordheim tunnelling (the graded barrier would considerably improve the operation [51]).

The system dynamics is presented by the phase diagram shown in figure 18; in this diagram, each thin horizontal line corresponds to a certain number of electrons trapped in the floating gate. To write digital unity into the cell, we apply positive voltage V_D to the word line and similar negative voltage $-V_D$ to both bit lines (see figure 17). Then some fraction α of the applied control voltage, $V_{ext} = \alpha 2 V_D$, drops between the floating gate and the word line, and exceeds the writing threshold V_t. The charge Q on the floating gate increases due to electron tunnelling to the word line, thus decreasing the voltage V_{fg-w} between them until $V_{fg-w} = V_t$ is reached.

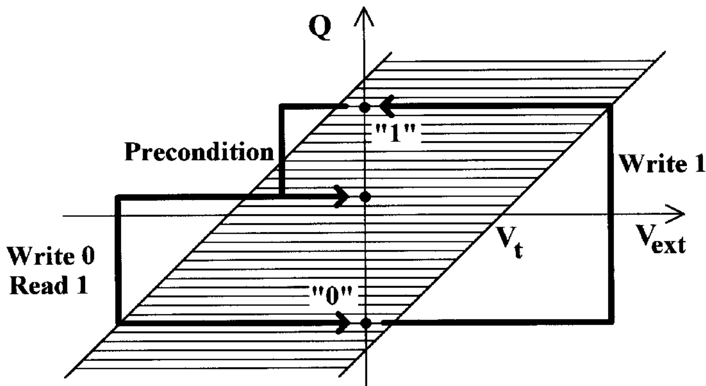

Figure 18. The phase diagram of the memory cell dynamics. Q is the charge of the floating gate while V_{ext} is the contribution to the voltage between the floating gate and word line due to external control voltage (between word and bit lines).

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(Actually, the Fowler–Nordheim tunnelling does not have a sharp threshold V_t. However, the voltage dependence is rather threshold-like allowing such an analysis.) The charge Q remains on the island after the applied voltage is removed (see figure 18). Writing of the digital zero is similar, with the change of the voltage polarity.

To read out the stored information we should try to write digital zero in, i.e. to apply positive voltage V_D to the bit lines and negative voltage $-V_D$ to the word line (small voltage difference $2V_r$ between two bit lines is used for the SET-transistor biasing—see figure 17). If digital zero has already been stored, the charge on the gate does not change, and the SET-transistor remains in the initial state. However, if digital unity has been stored on the gate, then its charge will gradually decrease down to the level corresponding to digital zero. During this decrease the current through SET-transistor performs several oscillations which are picked up by a FET sense amplifier. After rectification, this waveform is sent to the output, signalling that the selected cell had the state unity before the reading operation; if the state was zero, then no output signal is formed.

During the readout operation the voltage V_D is applied to the whole row of cells connected by the same bit lines. However, only the cell additionally selected by the voltage $-V_D$ on the word line should change its charge in the case if digital unity was stored. This condition defines the range of allowed threshold voltages V_t. To increase the parameter margins the cells can be preconditioned before reading by the application of a voltage V_D to the bit lines only (see figure 18) to remove the possible excess charge from neighbouring cells. The previously stored information is destroyed during readout, hence it should be restored later.

One FET may serve simultaneously a block of $N \gg 1$ SET cells connected in parallel. The maximum quantity is limited by the shot noise of SET-transistors [57] and depends on the operation frequency, number of stored electrons, and coupling between the SET-transistor and floating gate. Note that the principle of few-electron representation of a bit not only significantly increases the information retention time, but it is also necessary for the background-charge-insensitive operation of the SET-transistor.

The numerical estimates of the parameters of such a hybrid SET/FET memory have been done for the cell geometry presented in figure 19. The floating gate and the

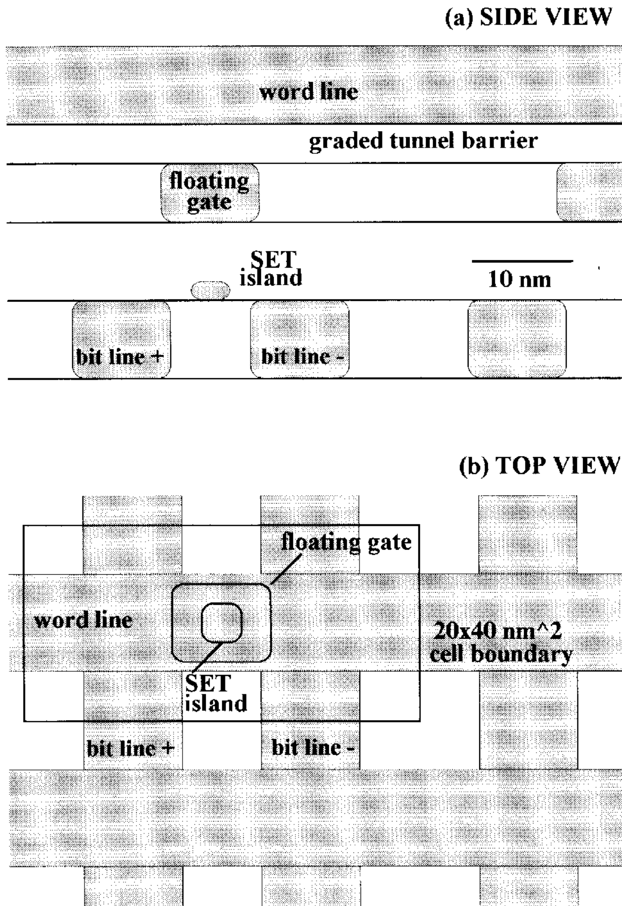

Figure 19. The proposed layout of the background-charge-insensitive memory cell [51].

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middle electrode of SET-transistor are assumed to be the islands of highly doped Si. It has been shown [51] that the density of 10^{11} bits/cm^2 and the room temperature operation of such a memory is feasible for $\sim$ 4 nm minimum feature size technology.

In this case the digital bit is represented by $\sim$ 10 electrons on the floating gate that corresponds to the change $\Delta Q_0 \sim 1.5e$ of the charge induced to the central electrode of SET-transistor during reading of digital unity. Estimated read/write time is about 3 ns and is limited both by the time of the floating gate charging and by the shot noise of the SET-transistor; the processes of charging the SET–FET interconnects ($\sim$0.1 ns) and of FET output lines ($\sim$1 ns) are considerably faster. For $N \sim 100$ SET-transistors in parallel the signal-to-noise ratio is about 10, which is still acceptable for a reliable readout. The total power dissipation ($\sim$3 W/cm^2) is mostly due to that in the FET sense amplifiers; power consumption of SETs ($\sim$30 mW/cm^2) and energy loss due to recharging of interconnects and floating gates ($\sim$3 mW/cm^2) are considerably lower.

The low-temperature prototype of such a background-charge-insensitive single-electron memory cell has been recently realized experimentally [33]. Instead of suggested positioning of the floating gate above the central island of SET-transistor, the

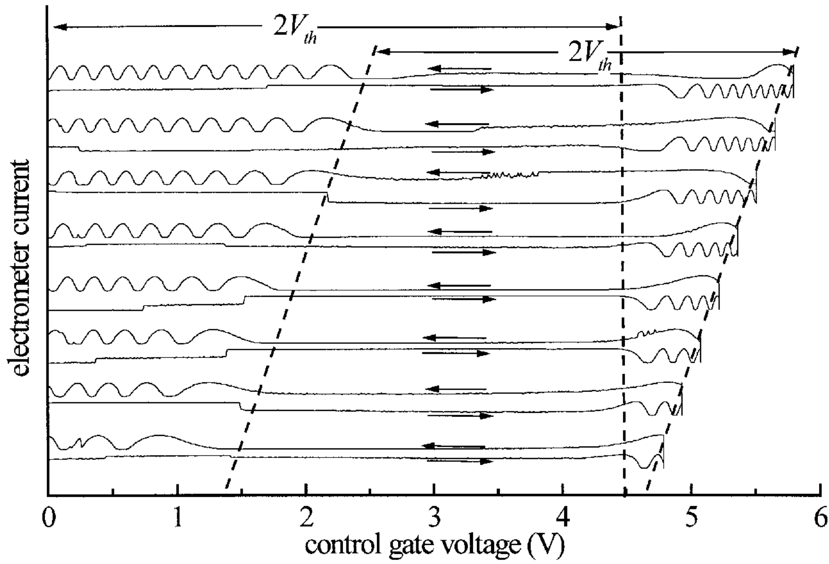

Figure 20. The operation of experimentally realized prototype [33] of the background-charge-insensitive memory cell (courtesy of C. D. Chen).

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planar geometry has been used (this reduces the coupling but does not influence the operation principle). The use of two control gates (which would correspond to one word line in figure 17) has allowed to compensate the direct influence of the control voltage on the charge induced to SET-transistor. As a result, the quasistatic readout becomes possible.

Figure 20 shows [33] the current through SET-transistor as a function of the control gate voltage (with the compensated direct influence) for several different sweeps of the control voltage (the SET-transistor bias voltage is fixed). The oscillations correspond to the change of the floating gate charge. When the negative sweep is started from the control voltage $V_{cg} = V_a$, at first there are no oscillations indicating that the charge of the floating gate does not change. Oscillations appear at $V_{cg} < V_b$ when the threshold of Fowler–Nordheim tunnelling is exceeded. The important observation is the almost constant difference $V_a - V_b$ for different starting points V_a as should be in an ideal case (compare with figure 18). The presence of oscillations for one sweeping direction and their absence for the other direction for the same control voltage (while there are no oscillations after the sweep reversing) shows that the device can be used as a memory cell. The operation obviously does not depend on the background charge of the SET-transistor.

The DRAM-type memory cell considered in this section is not the only possible application of the basic concept of background-charge-insensitive operation of the single-electron (actually few-electron) memory. For example, figure 21 shows the idea of a superdense (up to 10^{12} bits/cm^2) electrostatic storage disc [51]. Binary data may be written as few-electron charges in the ultrafine conducting grains (~1–3 nm) separated from conducting substrate by a ~5-nm-thick barrier, using the voltage pulse applied to a head (tip) moving close to the surface. Readout of the data may be performed with the same tip carrying the SET/FET transistor pair. The estimated bandwidth is up to 10^9 bit/s.

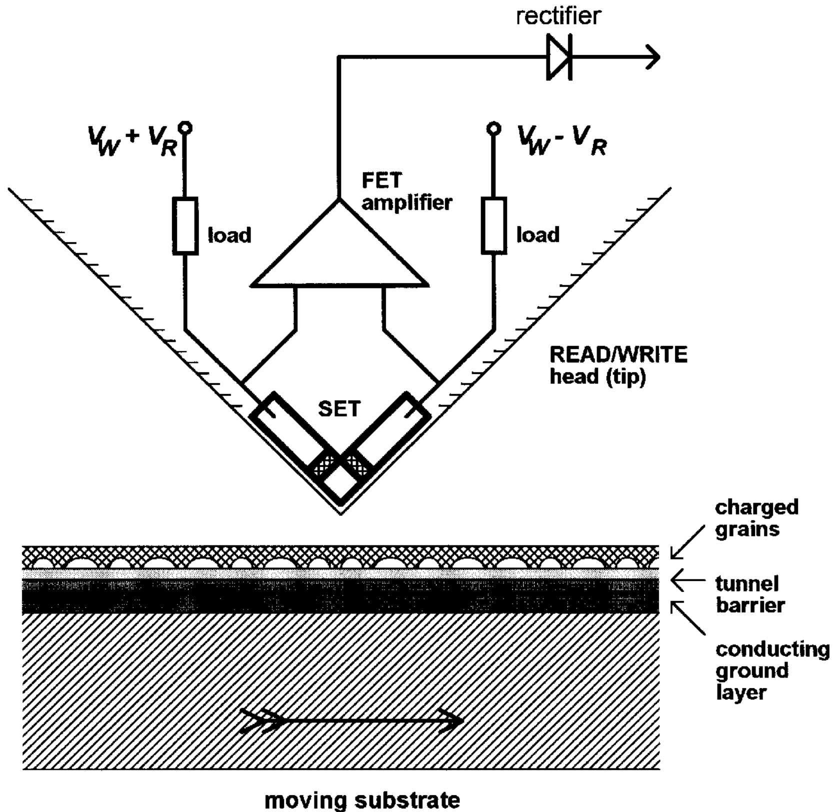

Figure 21. Electrostatic storage using SET readout [51]. The digital information is represented by few-electron charges of small conducting grains in the dielectric laver.

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9. Conclusion

At present the single-electronics can be considered as a leading candidate for future ultradense digital electronics which would be able to operate at the typical size scale of 10 nm and below, when the conventional principles will definitely not work. Nevertheless, the problems of digital single-electronics are very serious and still so far from being solved that the prospects of practical integrated devices are still uncertain.

The main problem remains to be the difficulty of fabrication of single-electron devices operating at room temperature. To achieve sufficiently small capacitances, the typical size of conducting islands should be on the order of a few nm. Such a fabrication technology is obviously not available at present and some indirect ways should be used for this purpose. Nevertheless, there is a rapid progress in the experiments with 'high-temperature' (up to room temperature) single-electron devices [18–23, 28–32]. Hopefully, with the further technological progress the room temperature devices will become routinely available.

The second major problem of integrated single-electronics which is especially important for logic circuits, is the random fluctuations of the background charge. Single-electron devices are so sensitive to the induced charge, that a single charged impurity in the close vicinity of a device can significantly influence its operation. In

the case of a single circuit, background charges can be adjusted individually with the help of additional gates. There is obviously no such possibility for integrated circuits.

There are a few potential solutions of this problem. First, there is some indirect experimental evidence [56, 89] that even in rather dirty systems the background charge tends to relax to zero. It can be hoped that the narrow statistical distribution of background charges might occur naturally in some materials. Second, it might be that the problem can be solved with the use of extremely pure materials. For example, considering molecular electronic devices in which all circuit elements are reproducible on the atomic level, there may be an extremely low concentration of impurities. Third, instead of capacitively coupled single-electron devices we can try to use resistively coupled circuits. For example, R-SET is not influenced by background charges at all. However, the problems are that R-SET is obviously much more difficult for fabrication than C-SET, and also the R-SET as a voltage amplifier requires significantly lower temperatures [90] because of the Nyquist noise in the coupling resistor.

Finally, the most radical solution of the background charge problem is to come up with some capacitively coupled devices which would work in the environment of fluctuating background charges. The particular idea of such background-charge-insensitive memory has been discussed in the previous section. However, although this idea can be used in the memory devices, it can hardly be applied to the logic circuits.

There are also other problems of integrated single-electron devices. For example, the high power dissipation is a common problem of any kind of ultradense digital devices. Assuming the density about 10^{11} cm^{-2}, the total heat generation becomes too large for the power dissipation as small as 10^{-10} W per elementary device.

In the paper we have discussed both single-electron logic and memory devices. From the parameter estimates one can see that the single-electron logic is much more difficult to implement than memory. All three problems mentioned above are significantly more severe for the logic. The room temperature operation of single-electron logic typically requires the size scale of conducting islands below 1 nm that could be accessible only for molecular electronics. The temperature limitation for single-electron memory is much softer. For example, the single-electron transistor can be used in memory circuits at temperatures more than five times higher than for a logic. The problem of fluctuating background charge has a clear solution so far only for memory devices. Finally, the power dissipation in memory circuits (excluding SRAM-type memory) can be considerably lower than in logic devices (except SET parametron-type circuits). This is because the information storage does not require power (only for refreshing of information in DRAMs) and at any particular moment only a small fraction of the whole device is used for writing and reading operations which require the power dissipation.

As a result, the integrated single-electron logic seems to be rather unrealistic for the implementation, at least in the near future. (Of course, it does not mean that its further study is meaningless. Moreover, the simple low temperature logic circuits can be demonstrated using present-day technology.) On the contrary, the prospects for the room temperature ultradense memory devices based on single-electron tunnelling are quite positive, that makes their experimental and theoretical study much more important from a practical point of view.

The single-electron digital devices are aimed to replace the conventional FET-based devices, because there should be a minimum size limit for the operation of the

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FET. However, it is still not clear what this size limit is. Recent experiments with SOI structures (see, e.g. [31, 32, 91]) and dual-gate transistors (see, e.g. [92]), and some theoretical studies [93, 94] indicate that FET-type structures could probably operate down to ~10 nm size scale. If these prospects become a reality, the single-electronics will be useful only at the size scale below 10 nm because the FET is obviously a simpler and more convenient device. Such a situation would also be beneficial for single-electronics because it would eliminate the large gap in the required minimal feature size between FET and SET electronics allowing smoother transition for the fabrication technology.

In recent experiments [31, 32] the memory cells with single-electron storage and FET-like sensing of the information have been realized (let us emphasize again that few-electron rather than one-electron representation of a bit seems to be more practical). In the ideas discussed in the previous section, the hybrid SET/FET circuits are used to solve the problem of relatively high output impedance of SET circuit. Generally, the combination of advantages provided by single-electronics and FET-type devices can be the major approach to the future ultradense digital devices.

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