Theoretical analysis of integrated single-electron memory operation

A.N. Korotkov, J.Appl.Phys. 92, 7291 (Dec. 2002)

Single-electron memory vs. single-electron logic

- Much simpler architecture for memory
- Passive information storage vs. active information processing
- Easier temperature requirements for memory
- Random background charge OK for single-electron memory

Single-electron memory is much simpler for implementation then single-electron logic

Various meanings of "single-electron memory"

- Bit representation by one electron (or few electrons)
- Coulomb blockade for information storage
- Read-out by single-electron transistor

Single-electron or few-electron bit representation?

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Advantages

- Fundamental limit
- Lowest energy dissipation
- Storage element as small as one atom
- No charging "tails" fi fast

Disadvantages

- Information destroyed by single leakage event
- Error probability grows linearly with time
- Refreshing impossible

Best case: single-electron storage (using single atoms?!) but extra redundancy (either few one-electron elements in one memory cell or check sums)

Single-electron Fowler-Nordheim tunneling

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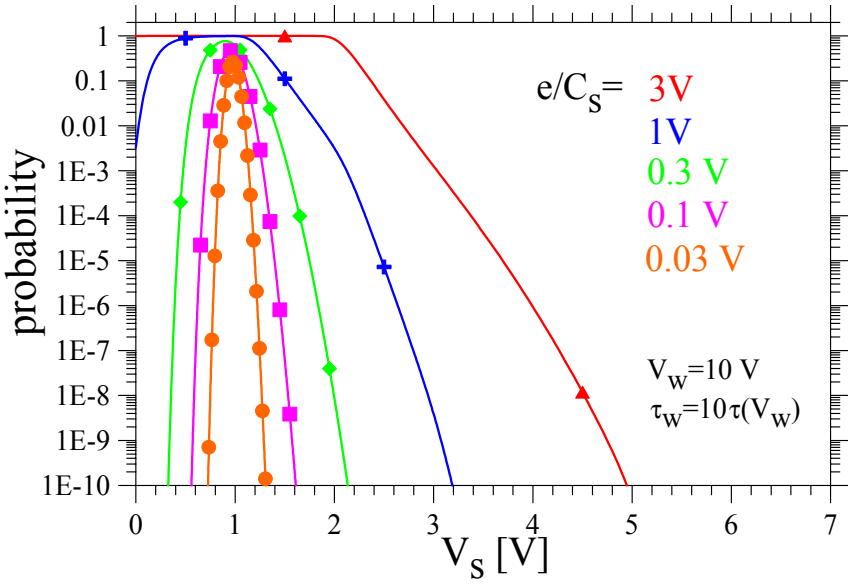
Probability distribution of floating gate potential after charging (solid line: random background charge, symbols: $q_0 = -e/2$)



Two possible regimes:

either many electrons (n>10) stored on the floating gate; random background charge OK,

or one electron; very long retention time for background charge $q_0 = -e/2$

Few-electron (2-10) regime is bad (fluctuations are too large)

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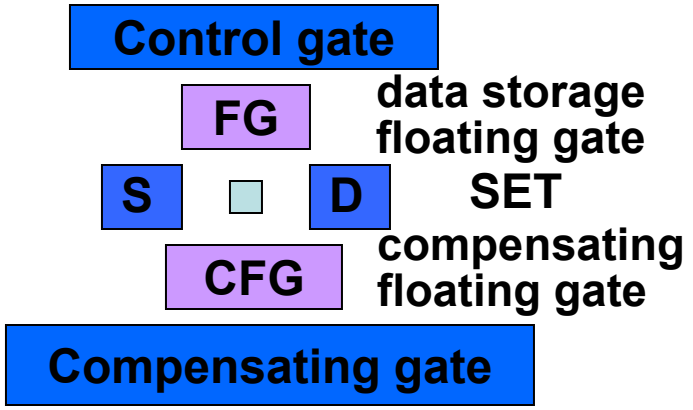
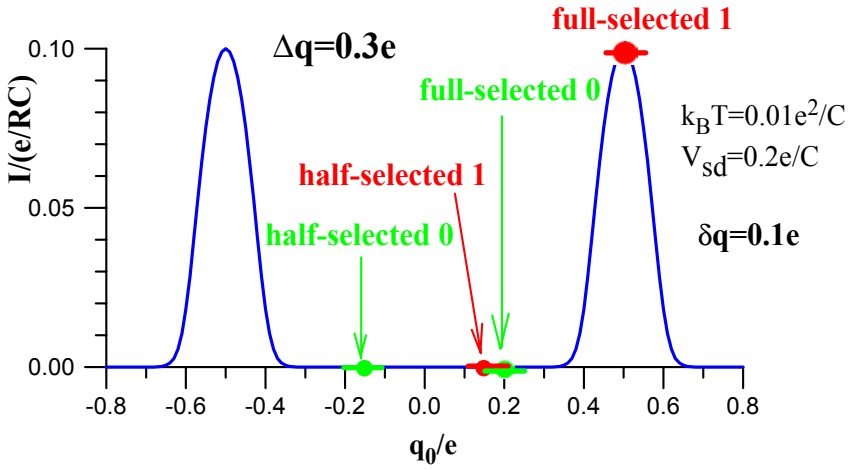
Background-charge-compensated SET readout



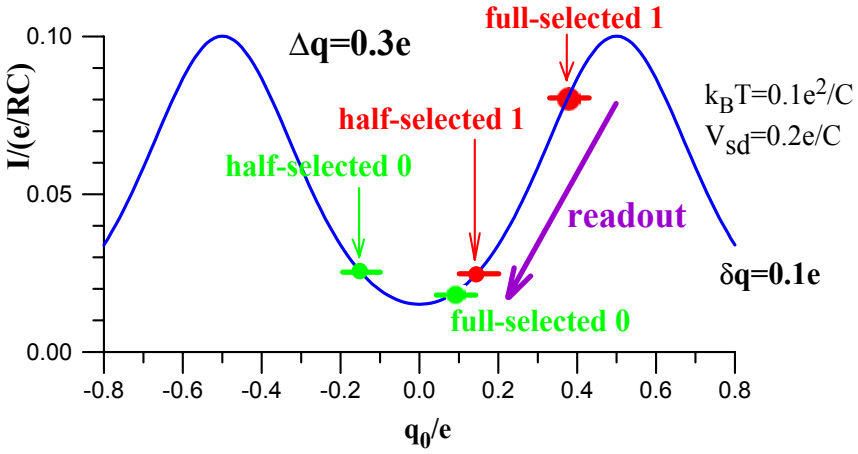
Nondestructive readout



SET operates as a switch

simpler

Destructive readout



signals before and after erase compared

better SNR, higher *T*

Defect-tolerant architecture based on nanofuses and nanoshorts

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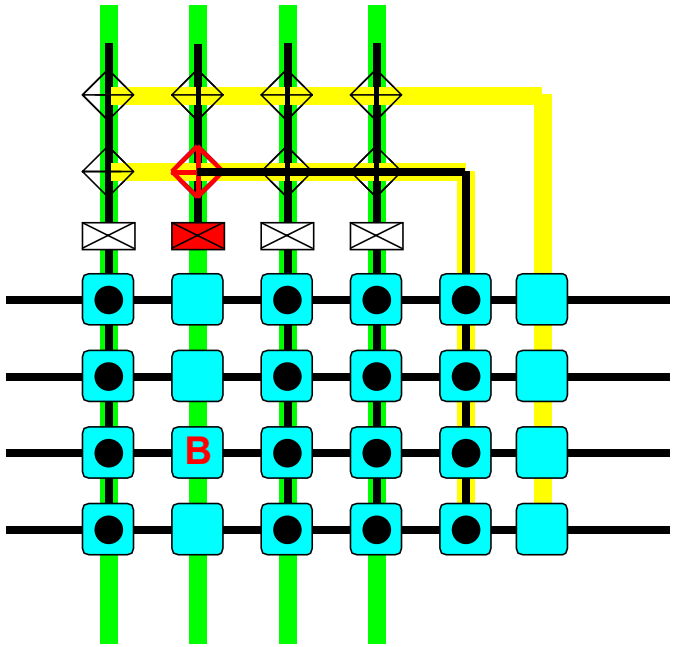
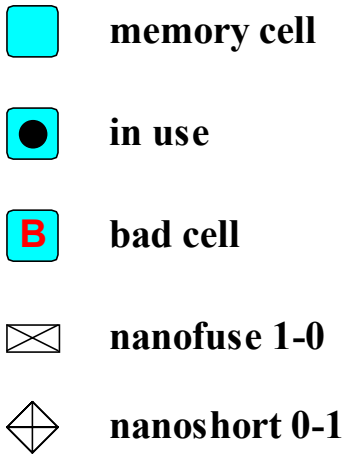
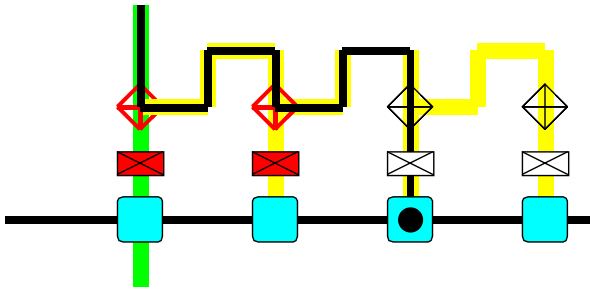
Idea: bit line rerouting by blowing nanofuses and activating nanoshorts

Needs reliable single-use nanofuses and nanoshorts (simple devices!)





Works even for low-yield cells:



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Calculating capacitance matrix by FASTCAP

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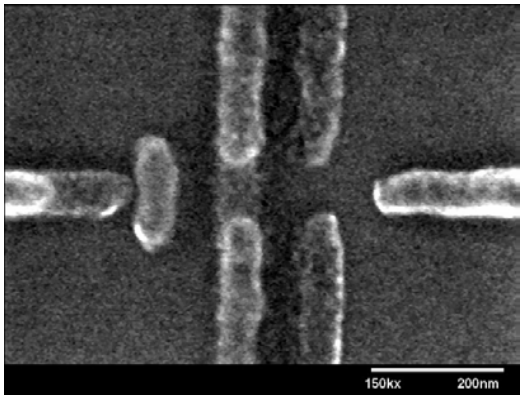
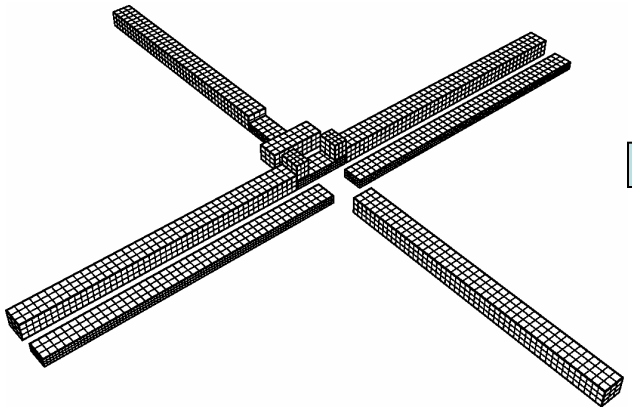
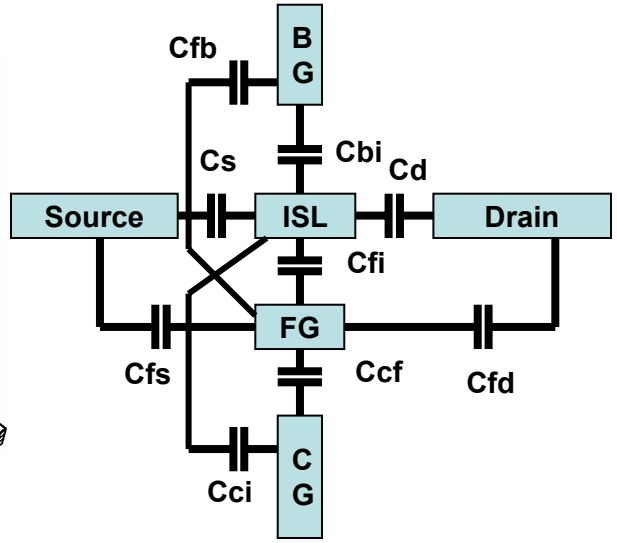


U. Notre Dame

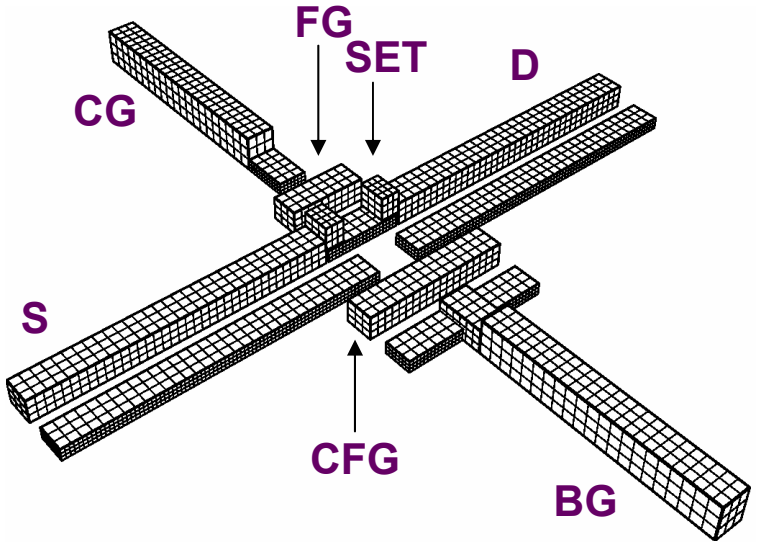


UC Riverside



	Cic,t	*Cib,t*	*Cfi/Cff*	*Vg* period
Theory	2.0 aF	0.69 aF	0.16	8 mV
ND exp	3.3 aF	0.73 aF	0.2	10 mV

Good agreement between theory and experiment



T-SPICE for SET circuits modeling

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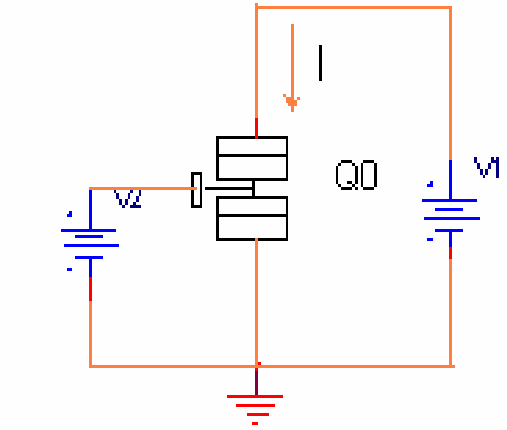

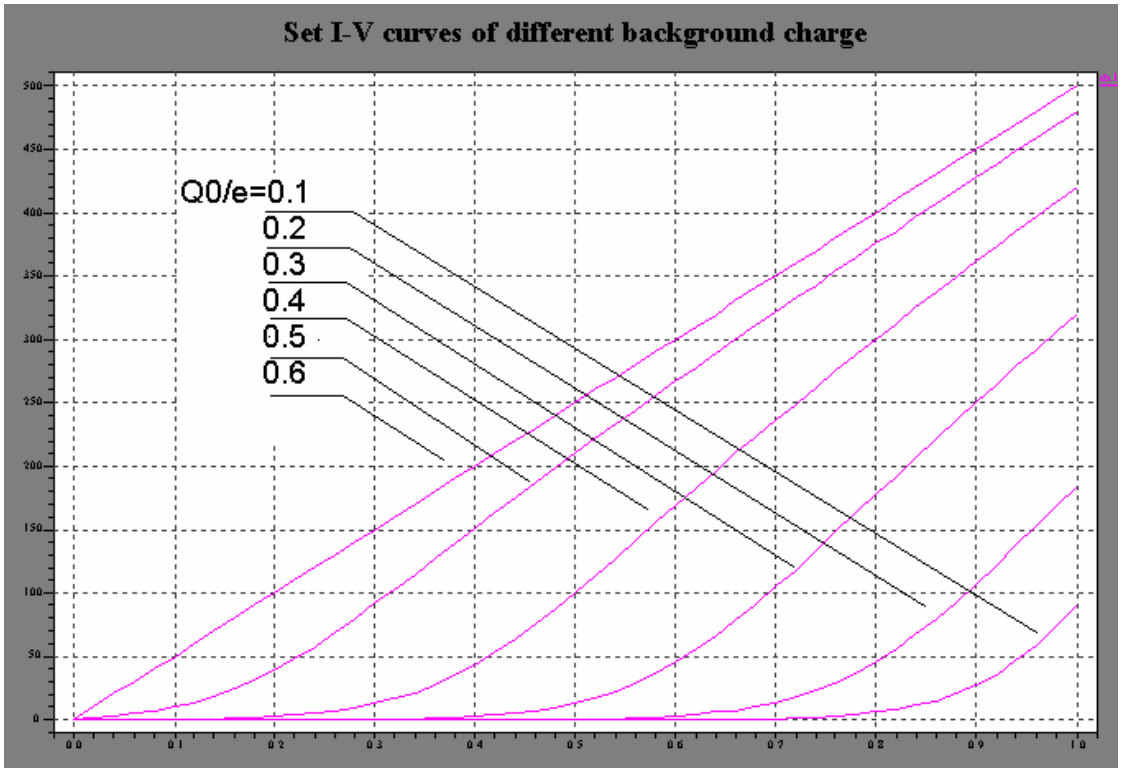

Full "orthodox" model for SET is used

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T-SPICE modeling results

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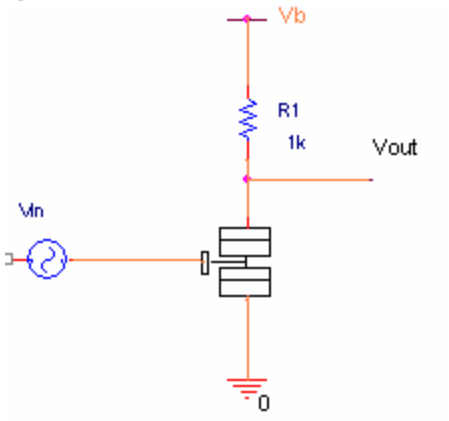
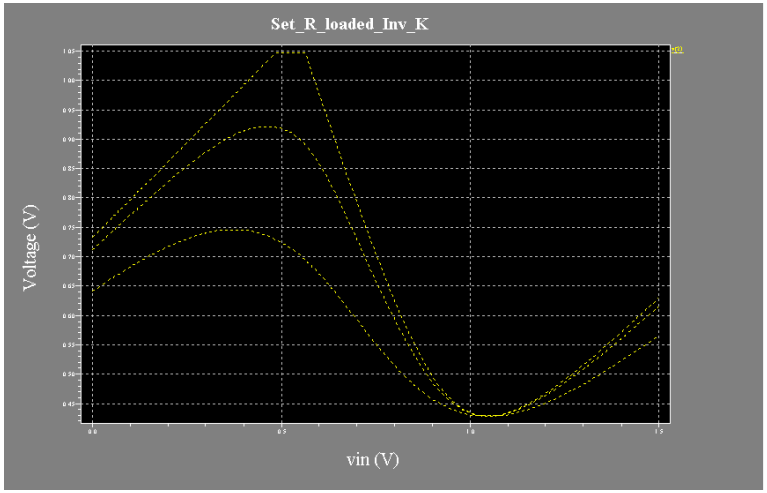
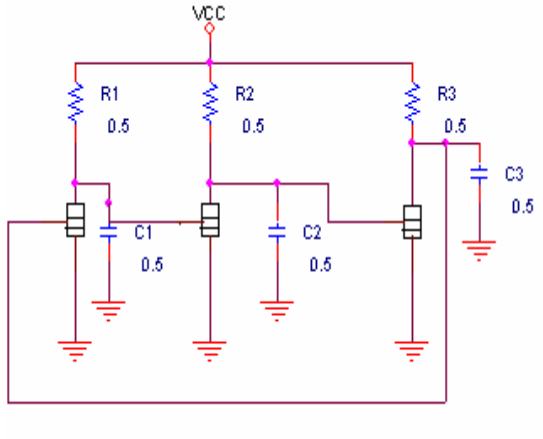
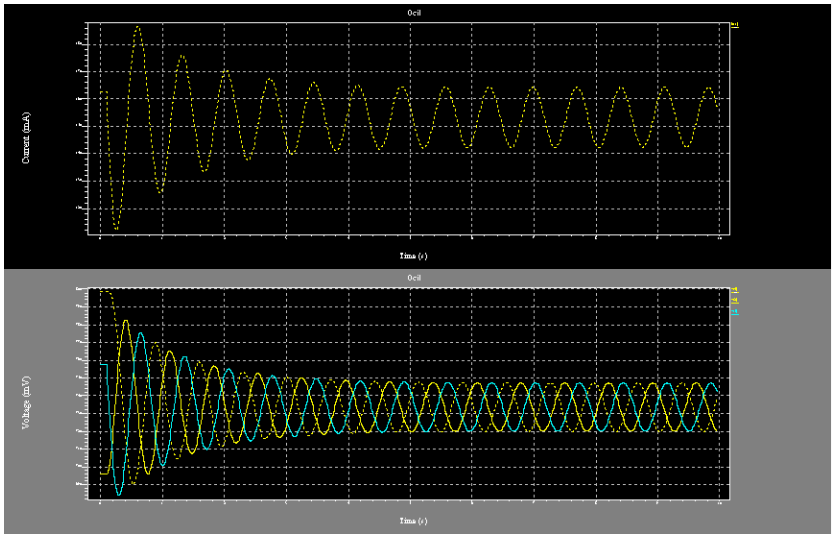
Resistively-loaded SET inverter





Ring oscillator with three SETs





T-SPICE works for SET circuits, but not very well

J. Yang, T. Gong, and A. Korotkov