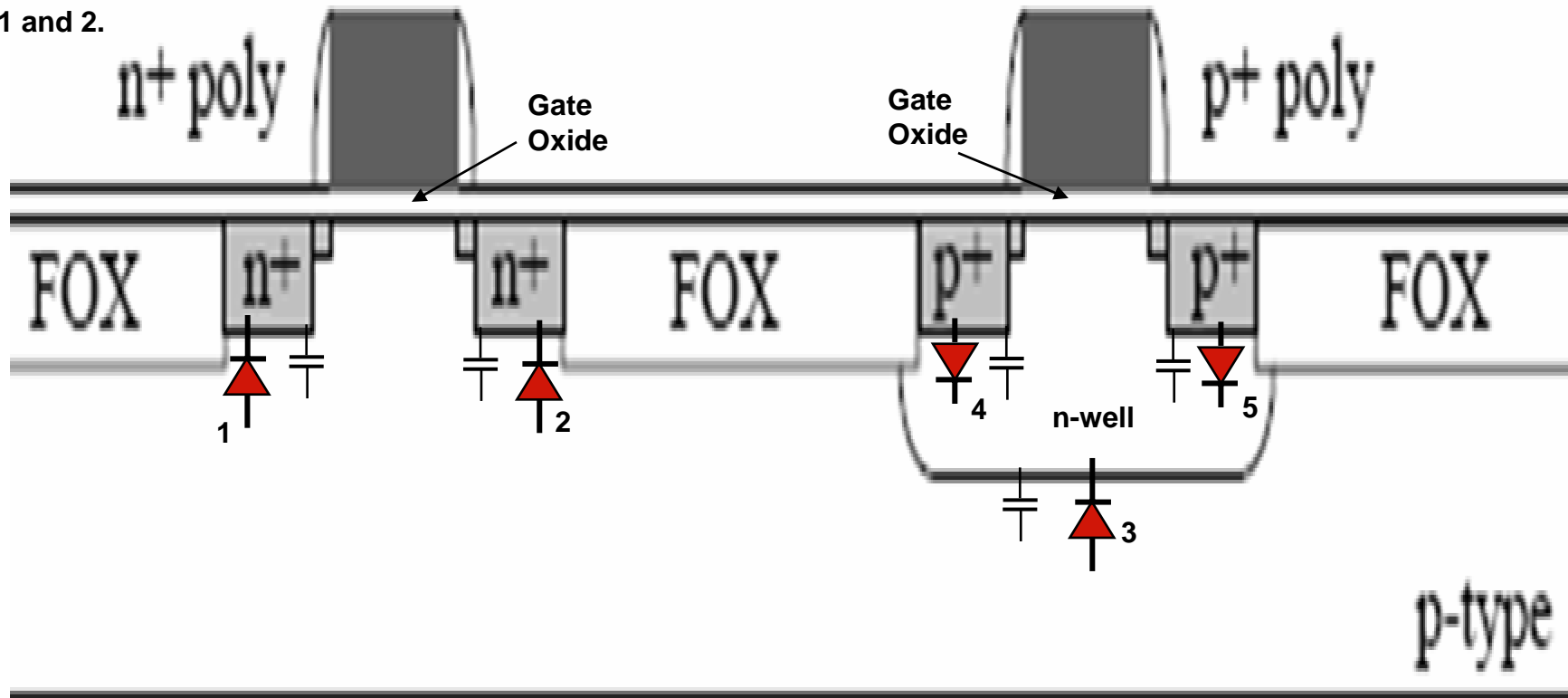


EE134 HW 1 Solution

1 and 2.



3. The p-type Si substrate should be at the lowest voltage on chip to keep diodes 1 - 3 reverse biased.
4. The n-well should be tied to the highest voltage on chip (V_{DD}) to keep diodes 3 - 5 reverse biased.
5. The electric fields are higher in the modern short channel transistor than in the long channel transistor because the voltages have not scaled down as fast as the spatial dimensions. At a high enough field, called the critical field (E_c), the velocity of the electrons or holes saturate and the FET enters into the velocity saturation regime. For $V_{GS} = V_{DD}$, the drain current of the modern FETS saturate due to velocity saturation. This occurs at a lower drain voltage V_{DS} than saturation in long channel FETs. In the velocity saturation regime, the drain current dependence on gate voltage is linear rather than quadratic as it is for long channel FETs in saturation.

$$6. \quad S = \frac{nk_B T}{q} \ln(10) \stackrel{n=1}{=} \begin{cases} 60 \text{ mV/dec @ } 27^\circ\text{C} \\ 74 \text{ mV/dec @ } 100^\circ\text{C} \end{cases} \quad \frac{I_{on}}{I_{off}} \Big|_{\max} = 10^{V_{DD}/S}$$

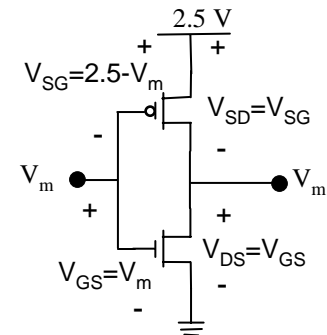
$$S(100^\circ\text{C}) = \frac{373.15}{300} S(300\text{K})$$

$$\frac{I_{on}}{I_{off}} \Big|_{\max} = 10^{V_{DD}/S} = \begin{cases} 10^{2.5/0.1} = 10^{25} \quad (T = 300\text{K}) \\ 10^{2.5/0.1244} = 1.26 \times 10^{20} \quad (T = 100^\circ\text{C}) \end{cases}$$

7. At the switching threshold, the voltages on the inverter are as shown at right.

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{\min} - \frac{V_{\min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

with $V_{\min} = \min(V_{GT}, V_{DS}, V_{DSAT})$



The unified model for the current from Fig. 3-23 is shown above. For the two cases of $V_m=1\text{V}$ and $V_m=1.5\text{V}$, we must determine V_{\min} using values from the table below.

Values to use from Table 3-2, p. 103. Note, in my convention, all PMOS voltages are positive.

	V_{TO} (V)	γ ($\text{V}^{0.5}$)	V_{Dsat} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	0.4	0.4	1.0	30×10^{-6}	0.1

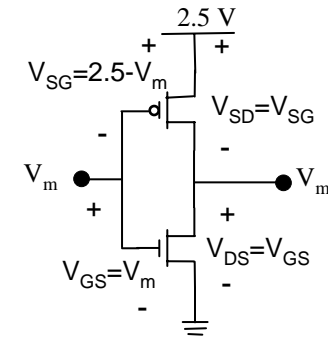
(a) $V_m=1V$

NMOS

$$\left. \begin{aligned} V_{GT} &= V_{GS} - V_{TN} = 1.0 - 0.43 = 0.57 \\ V_{Dsat,n} &= 0.63 \\ V_{DS} &= 1.0 \end{aligned} \right\} \Rightarrow V_{min} = V_{GT} = 0.57$$

PMOS

$$\left. \begin{aligned} V_{GT} &= V_{SG} - V_{TP} = 1.5 - 0.4 = 1.1 \\ V_{Dsat,p} &= 1.0 \\ V_{SD} &= 1.5 \end{aligned} \right\} \Rightarrow V_{min} = V_{Dsat,p} = 1.0$$



The NMOS is operating in charge saturation and the PMOS is operating in velocity saturation. (Sorry, I didn't realize this when I wrote the question). We might as well derive a general expression for W_p / W_n valid for all regions of operation. Since the two transistors are in series, their drain currents are the same. Therefore, we equate the two unified expressions for the current and rearrange to pull out the W_p/W_n ratios.

The drain current of the NMOS is,

$$I_D = k'_n \frac{W_n}{L_n} V_{min,n} \left(V_m - V_{Tn} - \frac{V_{min,n}}{2} \right) (1 - \lambda V_{DS,n})$$

And the drain current of the PMOS is,

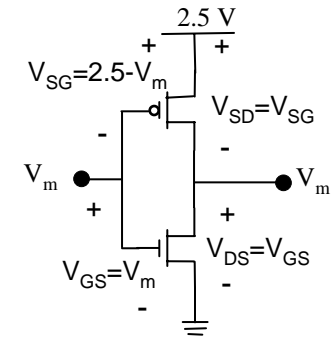
$$I_D = k'_p \frac{W_p}{L_p} V_{min,p} \left(V_{DD} - V_m - V_{Tp} - \frac{V_{min,p}}{2} \right) (1 - \lambda V_{SD,p})$$

Equating the two expressions and pulling out the W_p/W_n ratios gives

$$\frac{W_p/L_p}{W_n/L_n} = \frac{k'_n V_{min,n} \left(V_m - V_{Tn} - \frac{V_{min,n}}{2} \right) (1 - \lambda V_m)}{k'_p V_{min,p} \left(V_{DD} - V_m - V_{Tp} - \frac{V_{min,p}}{2} \right) (1 - \lambda (V_{DD} - V_m))}$$

Putting in all of the constants from Table 3-2 gives

$$\frac{W_p/L_p}{W_n/L_n} = \frac{115 \cdot V_{\min,n} \left(V_m - 0.43 - \frac{V_{\min,n}}{2} \right) [1 - 0.06 \cdot V_m]}{30 \cdot V_{\min,p} \left(2.5 - V_m - 0.4 - \frac{V_{\min,p}}{2} \right) [1 - 0.1 \cdot (2.5 - V_m)]}$$



Now plug and chug.

(a) $V_m = 1.0$, $V_{\min,n} = 0.57$, and $V_{\min,p} = 1.0 \rightarrow \boxed{W_p/W_n = 1.15}$

(b) $V_m = 1.5$, $V_{\min,n} = 0.63$, and $V_{\min,p} = 0.6 \rightarrow \boxed{W_p/W_n = 10.2}$

NMOS

$$\left. \begin{array}{l} V_{GT} = V_{GS} - V_{TN} = 1.5 - 0.43 = 1.07 \\ V_{Dsat,n} = 0.63 \\ V_{DS} = 1.5 \end{array} \right\} \Rightarrow V_{\min} = V_{Dsat,n} = 0.63$$

PMOS

$$\left. \begin{array}{l} V_{GT} = V_{SG} - V_{TP} = 1.0 - 0.4 = 0.6 \\ V_{Dsat,p} = 1.0 \\ V_{SD} = 1.0 \end{array} \right\} \Rightarrow V_{\min} = V_{GT} = 0.6$$