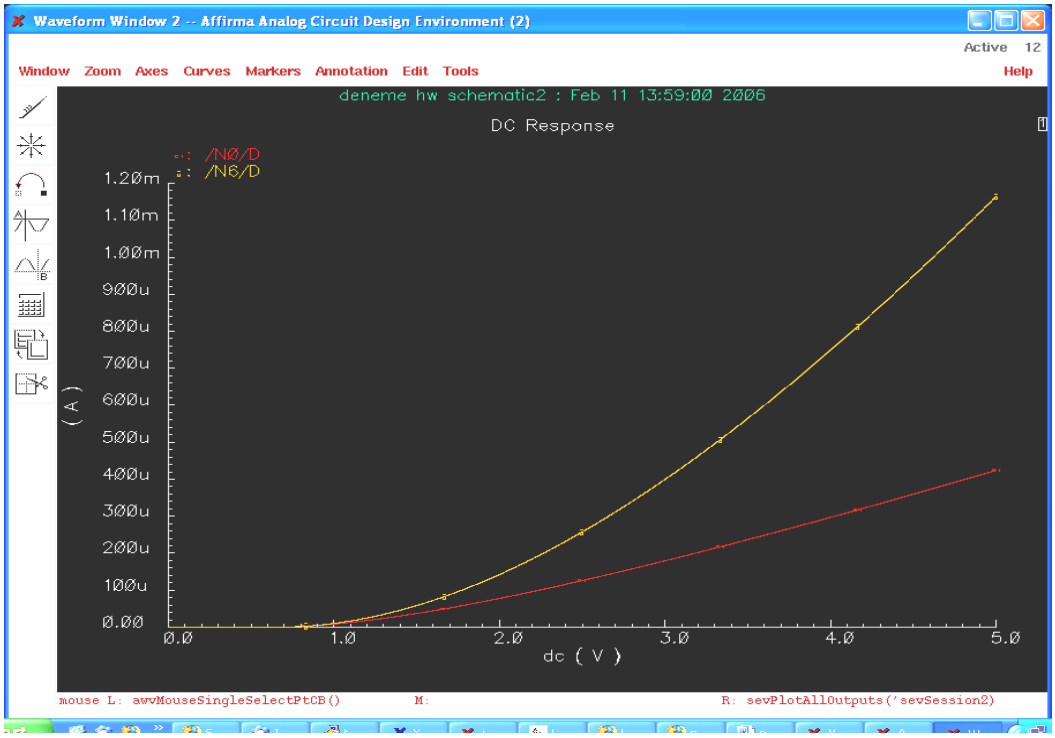
HW2 Solutions

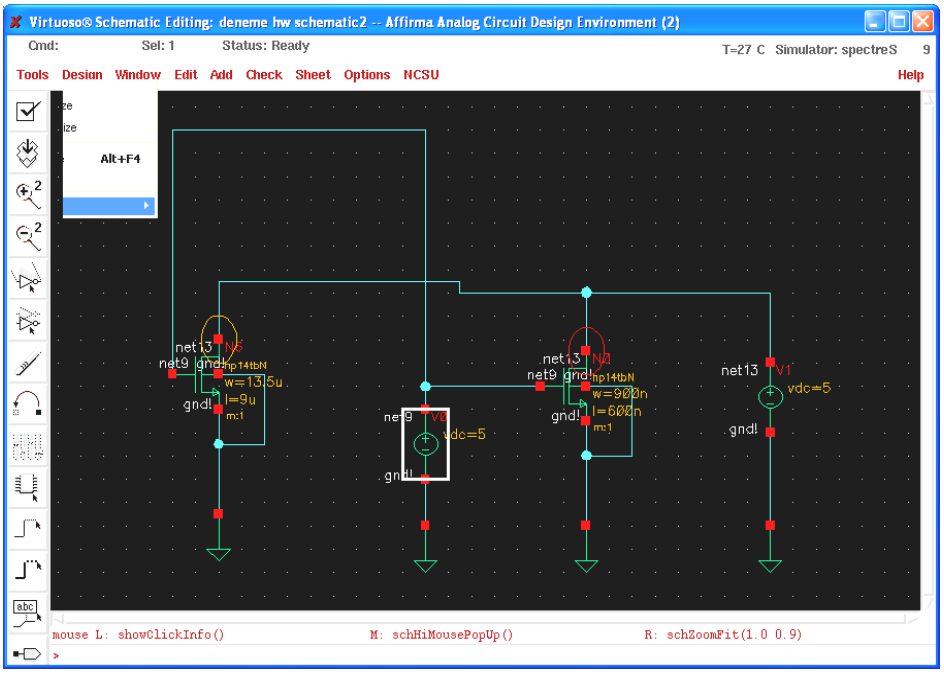
Q.1.

(a) The Given schematics will be generating the plots for the Long Channel and Short channel Ids-Vds characteristics with a DC sweep simulation in the Cadence Environment:

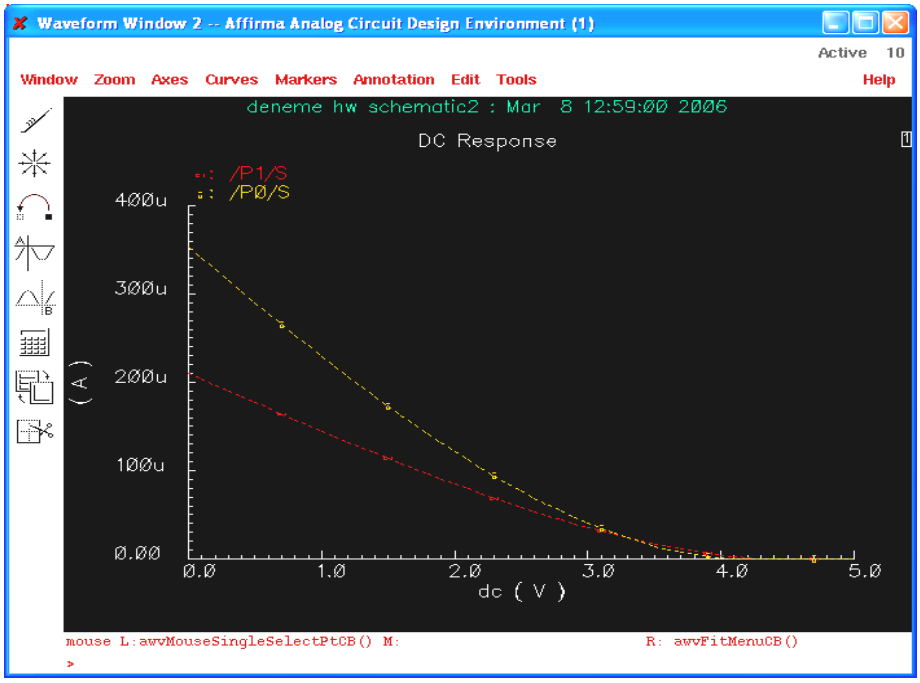


Ids vs Vgs for Vds= 5V, W/L=1.5. Red: L=0.6um, Orange: L=9um.

Schematics:

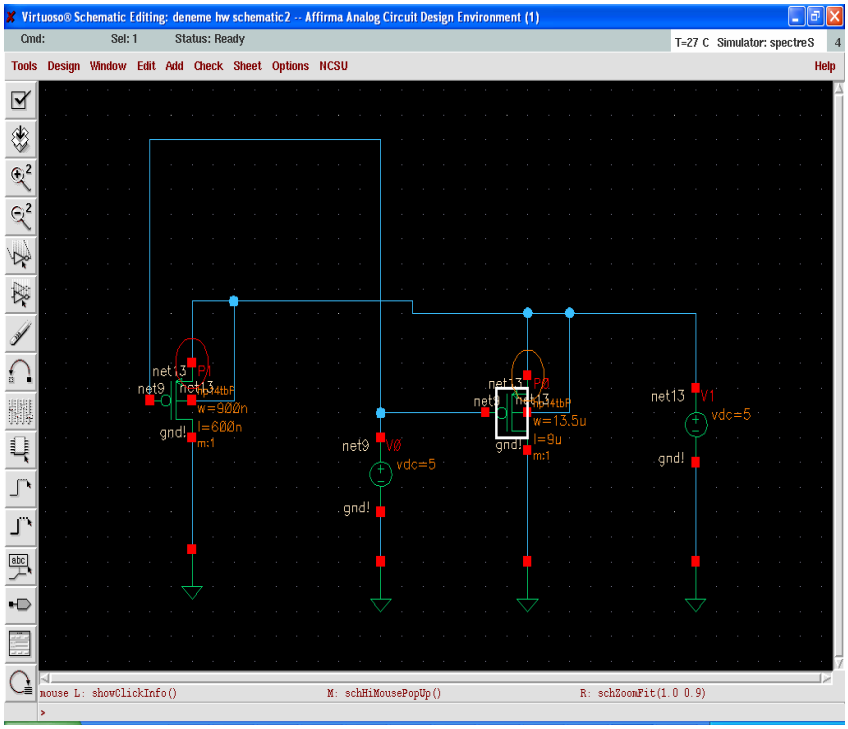


(b) Obtaining the plot for the PMOS transistor needs some consideration about the polarity of the current/voltage and the connection of the bulk terminal of the transistor. The bulk should be maintained at Vdd voltage in order to have operational transistors.



Isd vs Vsg for Vsd= 5V, W/L=1.5. Red: L=0.6um, Orange: L=9um.

Schematics:



Discussion:

Basically, short-channel transistor experiences the velocity saturation effect. For a short-channel device and for large enough values of V_{GT}, the device enter saturation before V_{DS} reaches V_{GS} - V_T. Therefore, the short-channel device experiences an extended saturation region, than the long-channel devices.

In SAT region, the devices can be simply modeled as:

Short-channel:

$$Id = v_{sat} C_{ox} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right) (1 + \lambda V_{DS})$$

Long-channel:

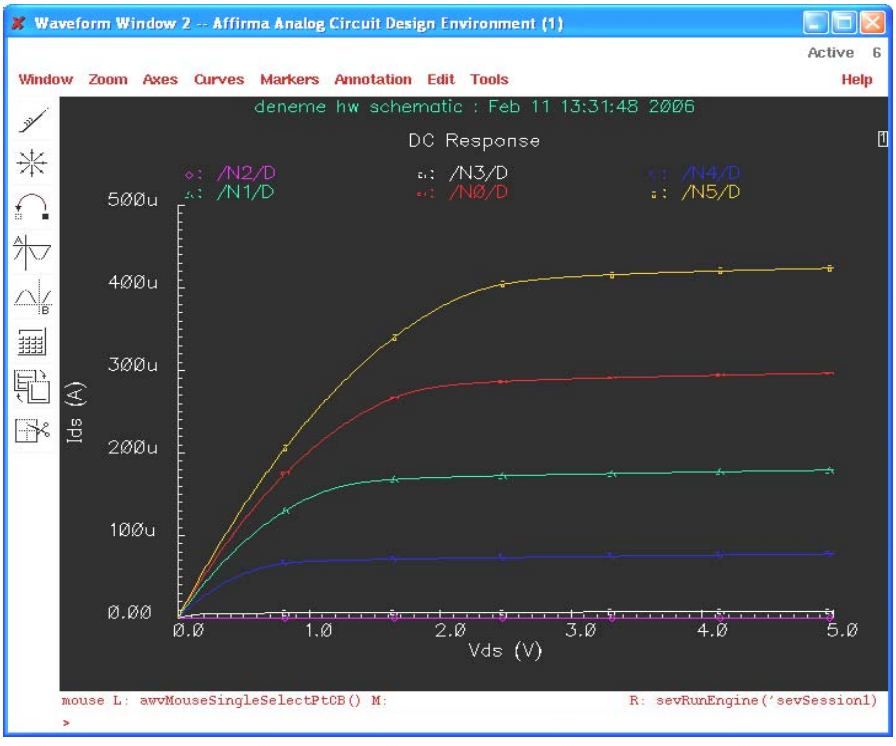
$$Id = \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

From these relations it is obvious that the drain current for short channel transistor has a linear dependence to V_{GS}, where the long channel device has a square dependence as observed in the simulations in part (a) and (b).

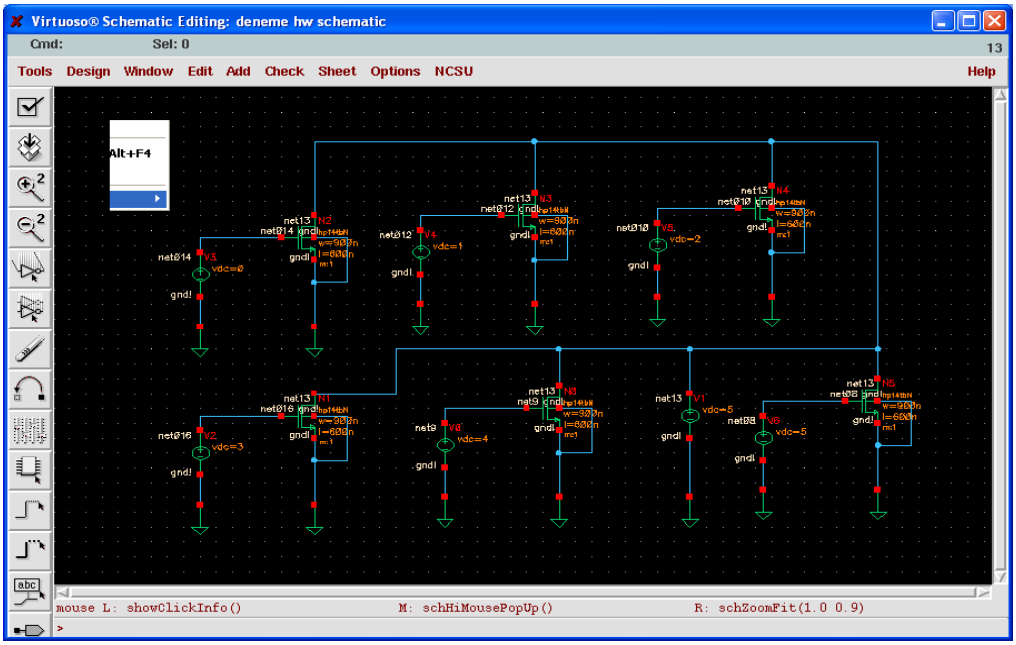
Q.2.

Simulations in the same manner for Vds sweep will result in the followings:

NMOS:

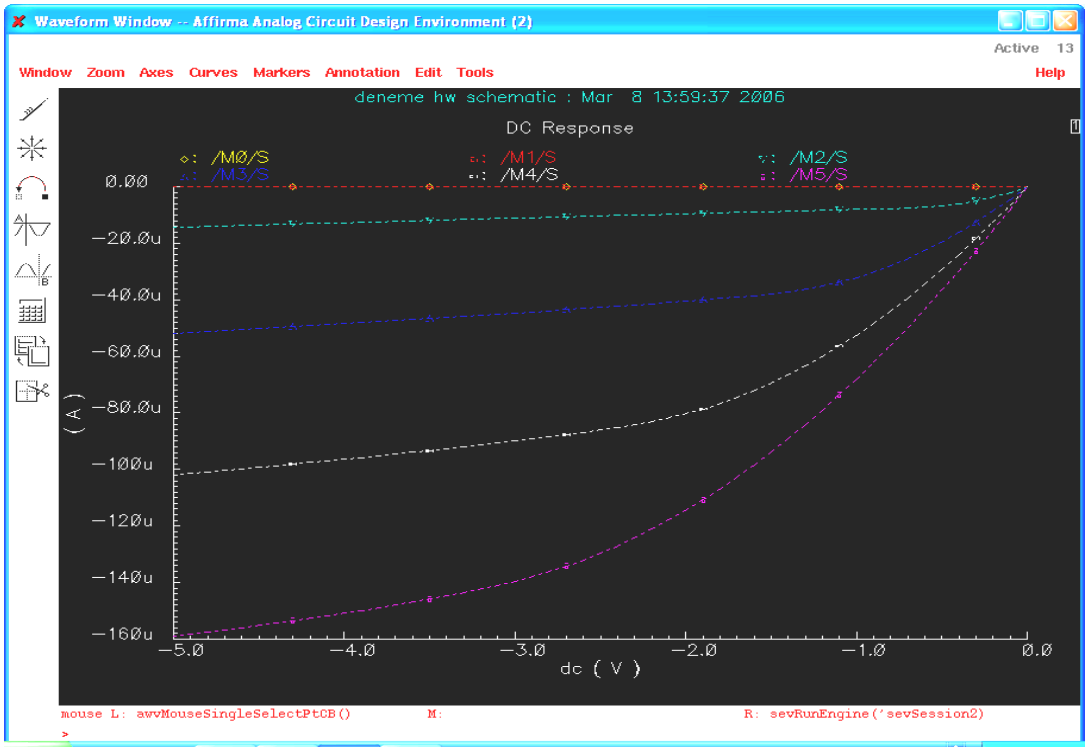


Schematic:

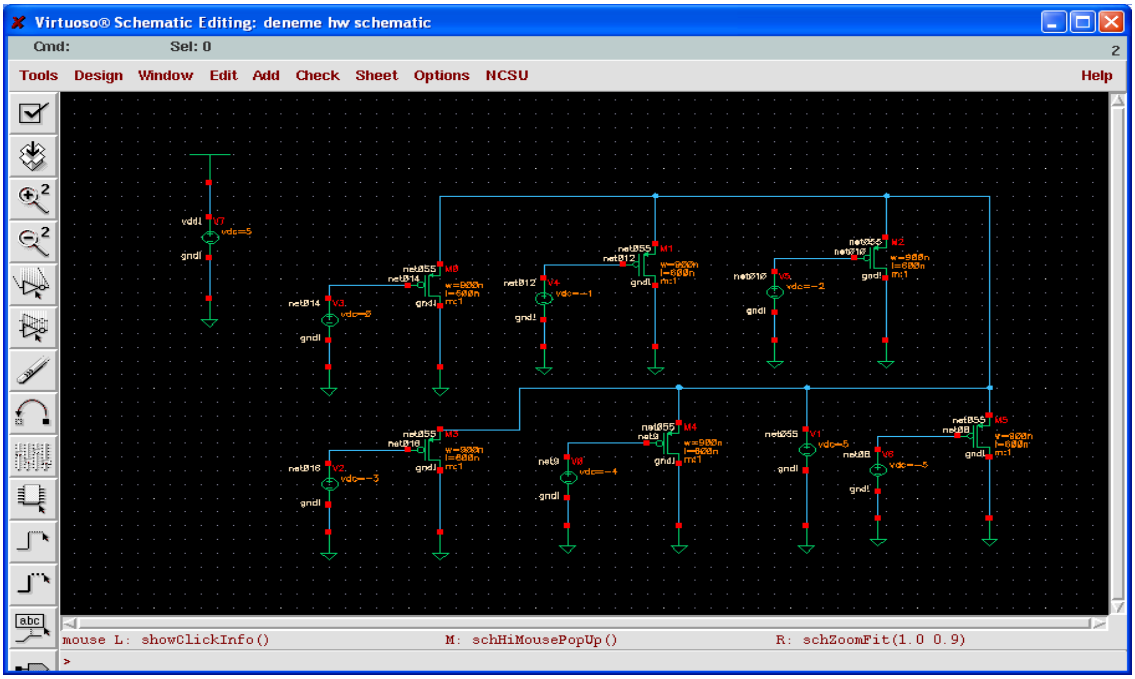


The design of schematics for the simulation is straight forward.

PMOS:



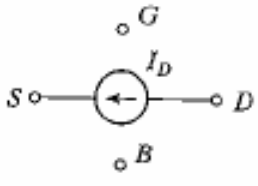
Schematics:



For the simulation of the PMOS transistors, the bulk connections should be made properly so that the transistors would be operating the correct regime. The bulks are all connected to Vdd = 5V in this case.

Q.3.

For this question you needed to upload your data you obtained from the question2 from Cadence to MATLAB. After this construction of the transistor model was required. For this purpose you had to create a table similar to the Table 3.2 in the text book. Then create your model in the MATLAB with a simple code. This code is written by following the model given in your text book:



$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{TO} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

Note that, the answer for this question is flexible as long as you have fitting curve with the Cadence data. However, as you expect, they should be converging to some specific values.

Parameters for the Transistors (W = 0.9um & L = 0.6um)

	Vt0	GAMMA	Vdsat	k'	lambda
NMOS	0.77	0.7483	2.205	4.59 E-05	0.03
PMOS	-0.77	-0.7483	-2.205	-1.36 E-05	-0.09

Your values should be in close neighborhood of these values.

Example Code:

NMOS:

```
%%%%%%%%%%%%%% Vgs = 5 %%%%%%%%%%%%%%


for i5 = 0:0.1:5

lamda = 0.03;
gamma = 0.7483559;
Vdsat =2.20583;
Vds = i5;
k = 0.459*10^-4;
w = 0.9;
l = 0.6;

Vgs = 5;

Vsb = -2.5;

phi = 0.45;
Vt0 = .76740855;
Vt = Vt0 + gamma*(sqrt(abs(-2*phi + Vsb))-sqrt(abs(-2*phi)));


Vgt = Vgs - Vt;

    if ((Vgt > Vds)&(Vdsat > Vds))
    Vmin = Vds;
        elseif ((Vds > Vgt) & (Vdsat > Vgt))
        Vmin = Vgt;
        else
        Vmin = Vdsat;
```

```
    end;

ID = k*w/l*(Vgt*Vmin- ((Vmin)^2)/2)*(1+lamda*Vds);

hold on;
plot (i5, ID, 'bo');
hold off;
    end;
```

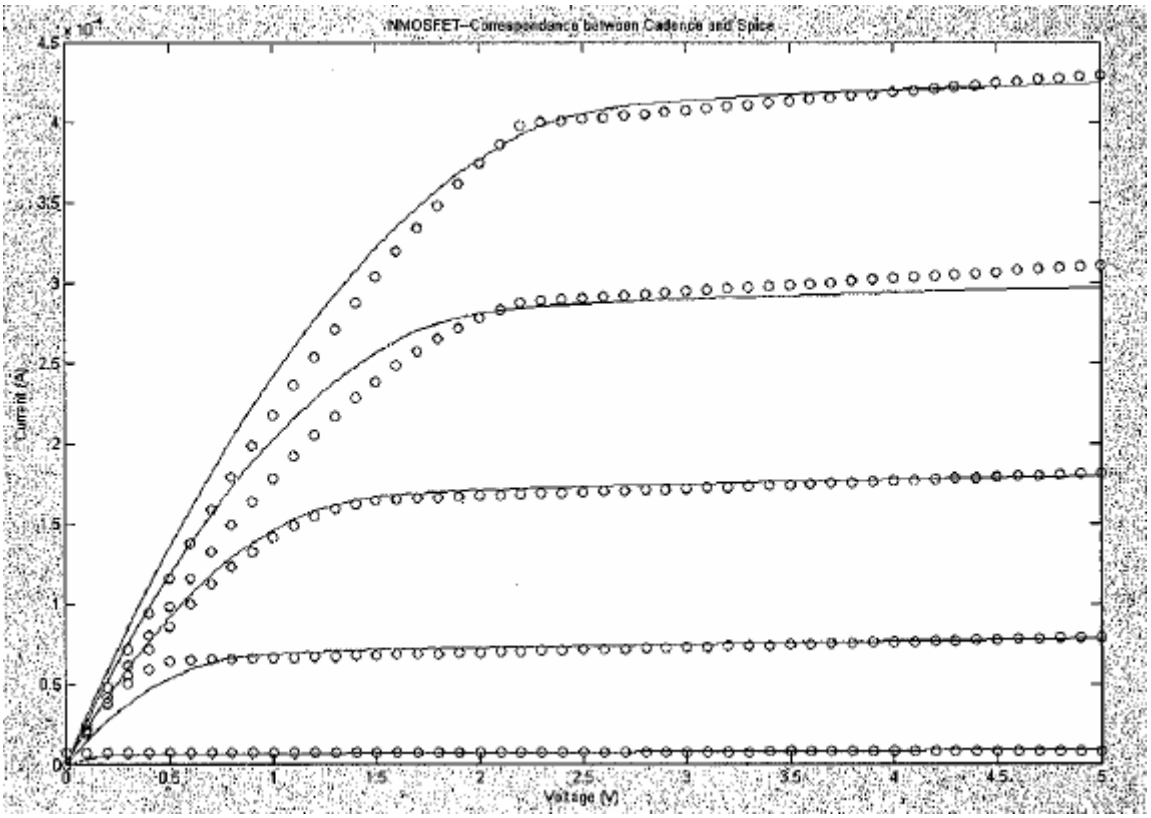
PMOS:

```
%%%%%%%%%%%%%%%%%%%%% Vgs = 5 %%%%%%%%%%%%%%%%%%%%%%%%%

for i5 = 0:0.1:5

lamda = 0.09;
gamma = 0.7483559;
Vdsat =2.20583;
Vds = i5;
k = 1.359*10^-5;
w = 0.9;
l = 0.6;

Vgs = 5;

Vsb = -2.5;

phi = 0.45;
Vt0 = .76740855;
Vt = Vt0 + gamma*(sqrt(abs(-2*phi + Vsb))-sqrt(abs(-2*phi)));


Vgt = Vgs - Vt;

    if ((Vgt > Vds)&(Vdsat > Vds))
    Vmin = Vds;
        elseif ((Vds > Vgt) & (Vdsat > Vgt))
        Vmin = Vgt;
```

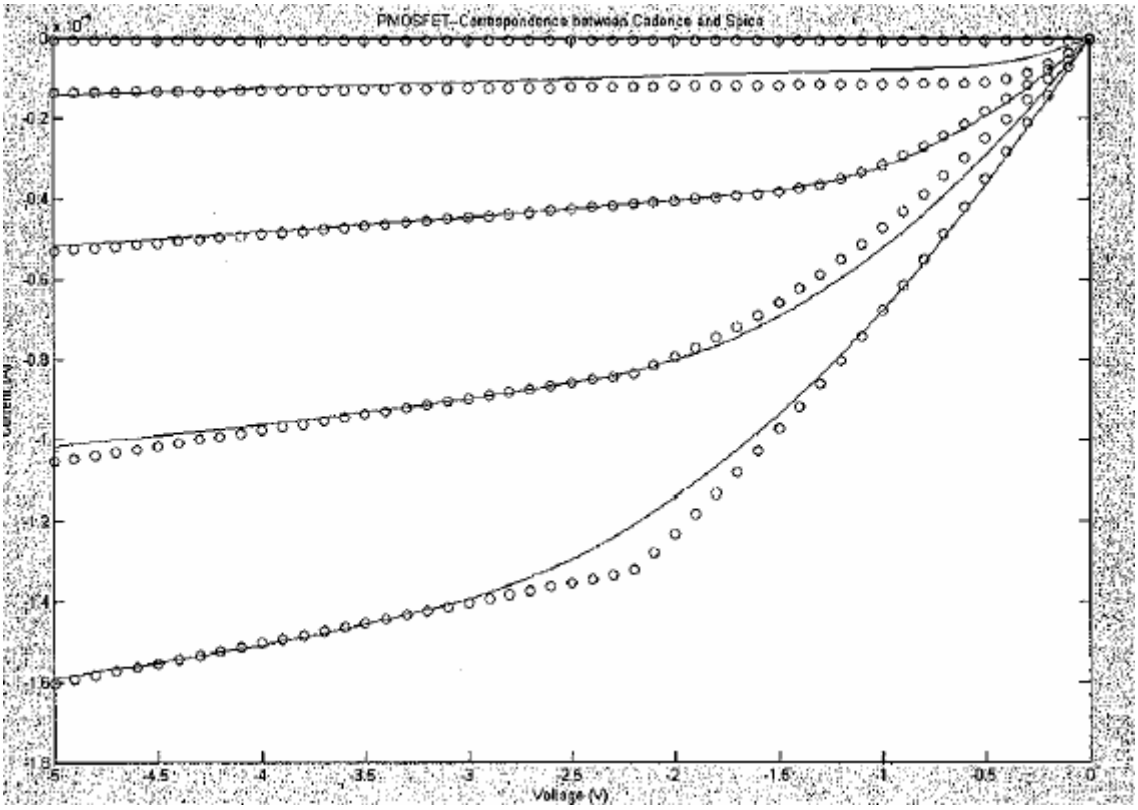
```
        else
        Vmin = Vdsat;
    end;

ID = -k*w/l*(Vgt*Vmin- ((Vmin)^2)/2)*(1+lamda*Vds);

hold on;
plot (-i5, ID, 'ro');
hold off;
    end;
```

The resultant waveforms are plotted on the waveforms imported from the Cadence:

NMOS:



PMOS:



Q.4.

In this question you needed to calculate the equivalent resistance for the transistor models that *you had created*.

Analytical Method:

$$R_{eq} = \frac{1}{-V_{DD}/2}\int_{V_{DD}}^{V_{DD}/2}\frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

$$\text{with}\quad I_{DSAT} = k'\frac{W}{L}\left((V_{DD}-V_T)V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})}+\frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right)\approx\frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

NMOS:

$$I_{DSAT} = 4.95E-5\frac{0.9}{0.6}\left((5-0.77)2.2-\frac{2.2^2}{2}\right) = 511.2\mu A$$

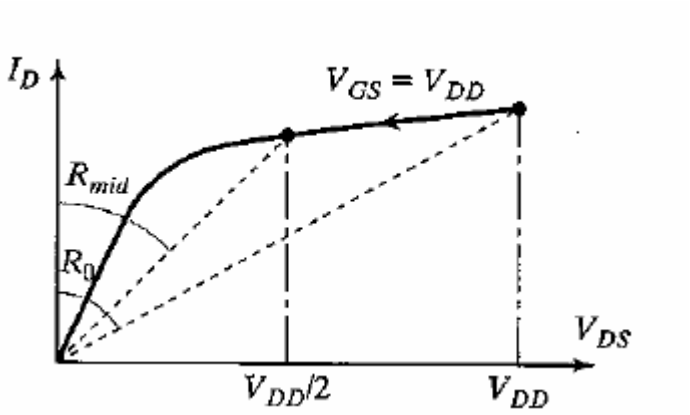
$$R_{EQ,N} = \frac{3}{4}\frac{5}{511.2E-06}\left(1-\frac{5}{6}0.03*5\right) = 6.4k\Omega$$

Simlarly for the PMOS:

$I_{DSAT} = 140.4\mu A$

$R_{EQ,P} = 16.7k\Omega$

Numerical Method:



As indicated in the question, we will get two points on the I-V curves and calculate R_{mid} and R_0. Average of two will give us an approximate value of the resistance of the transistor. (V_{DD} = 5 V)

NMOS:

$$R_0 = \frac{5}{4.3E-04} = 11.6k\Omega \qquad R_{mid} = \frac{2.5}{4.05E-04} = 6.1k\Omega \qquad R_{EQ,N} = \frac{R0+Rmid}{2} = 8.9k\Omega$$

PMOS:

$$R_0 = \frac{5}{1.6E-04} = 31.25k\Omega \qquad R_{mid} = \frac{2.5}{1.38E-04} = 18.1k\Omega \qquad R_{EQ,P} = \frac{R0+Rmid}{2} = 24.6k\Omega$$