EE134 HW 3 Solution

1.Delay time through an inverter:

Calculate the average propagation delay time (t_p) through a minimum size inverter driving an identical minimum size inverter using the example process of the text. This corresponds to an inverter similar to Fig. 5-15. The difference is that both the NMOSFET and PMOSFET have W/L = 0.375 / 0.25.

a. For the PMOS, scale the values for the capacitances in Table 5-2.

b. Determine the appropriate values of Req,p and Req,n.

c. Determine t_{pHL}, t_{pLH}, and t_p.

a. In Table 5-2, all capacitances (except the wire capacitance, C_w, are proportional to the width of the transistors. The values in Table 5-2 are for the NMOS and PMOS of Fig. 5-15. The NMOS width is 0.375 μm and the PMOS width is 1.125 μm. Therefore, we need to scale the capacitance values for the PMOS, i.e., $C_{new} = (W_{new} / W_{old}) C_{old}$ or for a specific example $C_{gd2} = 0.61 (0.375 / 1.125) = 0.203$ fF. The values for transistors 2 and 4 get modified, so that Table 5-2 becomes

Capacitor	(H ➔ L) (fF)	(L➔ H) (fF)
Cgd1	0.23	0.23
Cgd2	0.203	0.203
Cdb1	0.66	0.9
Cdb2	0.5	0.383
Cg3	0.76	0.76
Cg4	0.76	0.76
Cw	0.12	0.12
CL	**3.233**	**3.356**

b. The resistances in Table 3-3 are for the minimum L = 0.25 μm and for W = L. The resistances are proportional to (1/W), so

$R_{eq,n} = 13 (0.25 / 0.375) = 8.67$ kΩ.
$R_{eq,p} = 31 (0.25 / 0.375) = 20.67$ kΩ.

c. $t_{pHL} = 0.69 R_{eq,n} C_L$(H➔L) = 0.69 (8670) (3.233e-15) = 19.34 ps.
$t_{pLH} = 0.69 R_{eq,p} C_L$(L➔H) = 0.69 (20.67e3) (3.356e-15) = 47.86 ps.
$t_p = (t_{pLH} + t_{pHL}) / 2 = 33.6$ ps.

2. Design a chain of inverters to drive a large capacitive load:

The output of an inverter sized as shown in Fig. 5-15 must be sent to an output pin with a capacitance of 20 pF. The average maximum delay is specified to be less than 2 ns. Design an inverter chain that uses the fewest number of inverters and still meets the delay specification. Use parameters for the example process of the text.

This is identical to the problem that we did in lecture. In the lecture, we showed that for N=7, $t_{p,min}$ = 0.5 ns, for N=4, t_p = 0.63 ns; for N=3, t_p = 0.95 ns; and for N=1, t_p = 107 ns. Now we need to check whether N=2 will work. The equation that we use is $t_p = t_{p0} N (1 + f/\gamma)$.

N is the number of inverters,
γ is the ratio of the internal or intrinsic capacitance to the gate capacitance and is very close to 1.0. We calculated it to be 0.97 and I will use 1.0 for these calculations.
t_{p0} is the intrinsic delay time resulting from the intrinsic inverter capacitance (no load capacitor).
$f = [C_L / C_{in1}]^{1/N}$ where $C_{in1} = C_{gp1} + C_{gn1}$.

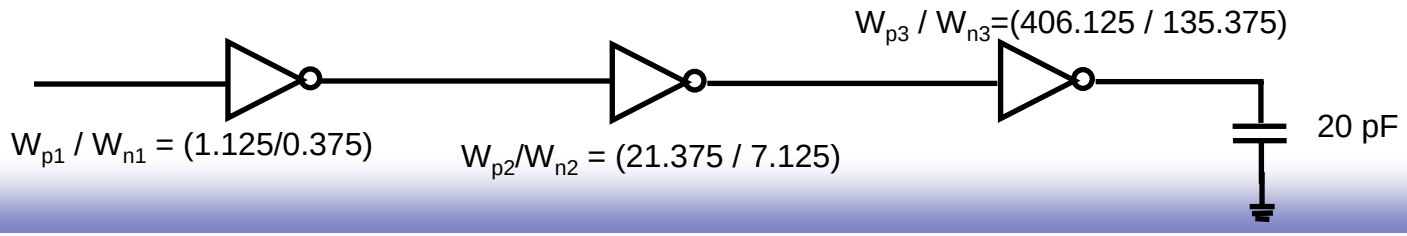
From Table 5-2, C_{in1} = 3.04 fF, $C_{int,HL}$ = 3.0 fF, and $C_{int,LH}$ = 2.89 fF. From Table 3-3, $R_{eq,n}$ = 13 / (3/2) = 8.67 kΩ and $R_{eq,p}$ = 31 / (9/2) = 6.89 kΩ. Therefore,

$t_{pHL,0}$ = 0.69 (8.67e3) (3.0e-15) = 1.79e-11 s, $t_{pLH,0}$ = 0.69 (6.89e3) (2.89e-15) = 1.37e-11 s, and $t_{p0} = (t_{pLH,0} + t_{pHL,0})/2$ = 1.584e-11 s.

$f = [20e\text{-}12 / 3.04e\text{-}15]^{1/2}$ = 81.11 = 81 rounding off to the nearest integer.

So, for N=2, $t_p = t_{p0} N (1 + f/\gamma)$ = 1.584e-11 (2) (1 + 81) = 2.6e-9 = 2.6 ns. This does not meet spec, so the answer is N=3 which we did in class.

For N=3, f = 19. Therefore, the inverter chain consists of 3 inverters starting with the (1.125/0.375) inverter of Fig. 5-15 with the gate width of each successive inverter increasing by a factor of 19. $W_{p2}/W_{n2} = 19 (W_{p1} / W_{n1})$ = (21.375 / 7.125). $W_{p3} / W_{n3} = 19^2 (W_{p1} / W_{n1})$ = (406.125 / 135.375).



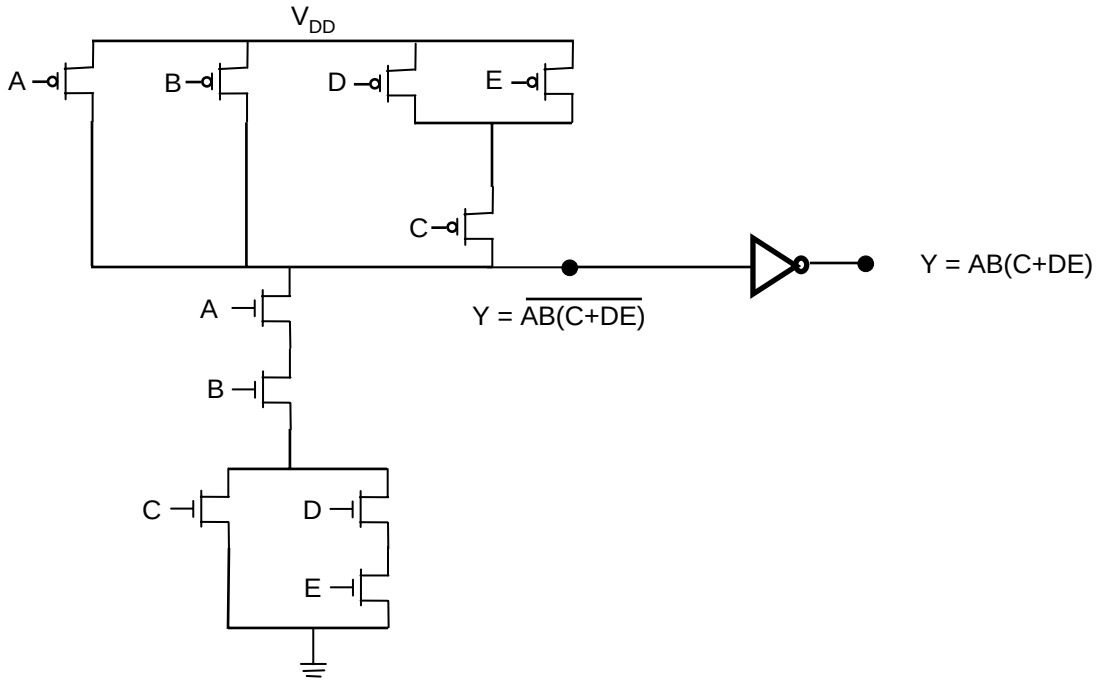
3. Design a static complementary CMOS logic gate:

Design a complementary CMOS logic gate to implement the logic Y = AB(C+DE). (you can assume that you will have an inverter available at the output).

a. Draw the circuit schematic so that there is minimum capacitance at the output node.

b. Assuming all minimum size inverters (identical to that in problem 1), calculate the worst case t_{pHL} and t_{pLH} for C_L = 50 fF neglecting all other capacitance. Use the first order approximation that we used in class of 0.69 R_{eq} $C_{L.}$

a.



b. t_{pHL} = 0.69 $R_{eq,n}$ (50e-15). For worst case, we pull down through 4 NMOS transistors in series. $R_{eq,n}$ = 4 (8.67 kΩ) = 34.68 kΩ. So t_{pHL} = 0.69 (34.68e3) (50e-15) = 1.20 ns.

t_{pHL} = 0.69 $R_{eq,p}$ (50e-15). For worst case, we pull up through 2 PMOS transistors in series. $R_{eq,p}$ = 2 (20.67 kΩ) = 41.34 kΩ. So t_{pLH} = 0.69 (41.34e3) (50e-15) = 1.43 ns.