# Digital Integrated Circuit (IC) Layout and Design - Week 10, Lecture 20

- Midterm Due in Class
- Dynamic Logic
- SRAM
- Wrap up

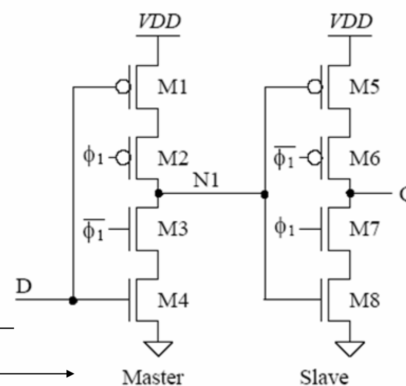


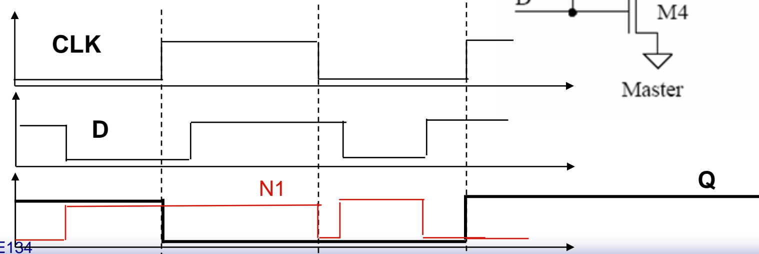
# Clocked CMOS Logic ($C^2MOS$)

## Clocked CMOS Register (Positive Edge)

$\phi_1$ low:
- Master enabled. N1 = $\overline{D}$. M1 & M3 on.
- Slave latched. M6 and M7 off. Output Q is in charge storage mode (floating). Hi-Z state (high impedance).

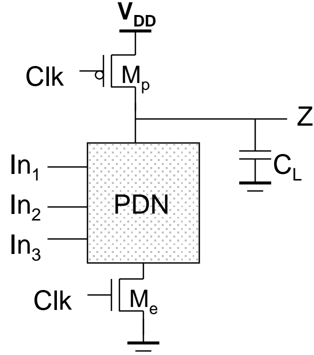
$\phi_1$ high:
- Master Hi-Z state (N1 floating $\overline{D_n}$).
- Slave enabled. $Q_{n+1} = D_n$.



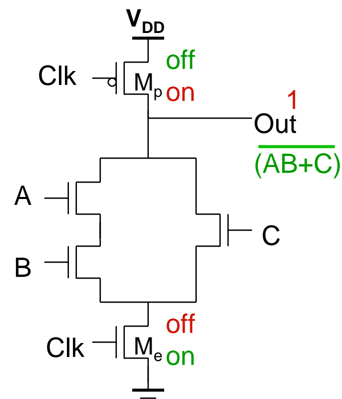



# $C^2$MOS: Precharge – Evaluate (PE) Logic

**General Concept**




**Specific Example**




**CLK = 0**: Precharge output Z = $V_{DD}$.
$M_e$ off; $M_p$ on. Z = $V_{DD}$.

**CLK = 1**: Evaluate. $M_p$ off. $M_e$ on.
Pull down Z (or not) depending on logic implemented in PDN.

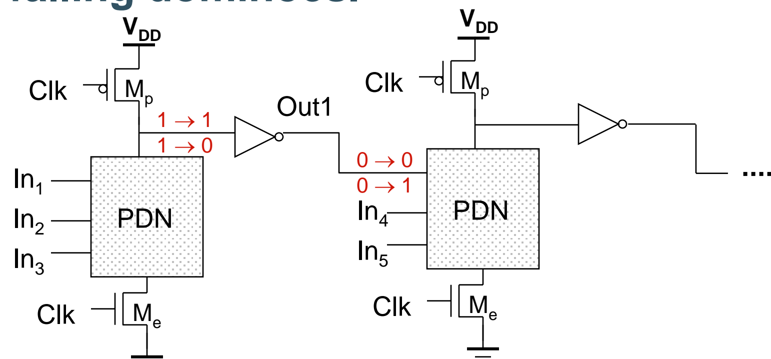
**CLK = 0: Precharge Z = 1**

**CLK = 1: Evaluate. Z = $\overline{(AB + C)}$**



# Domino Logic

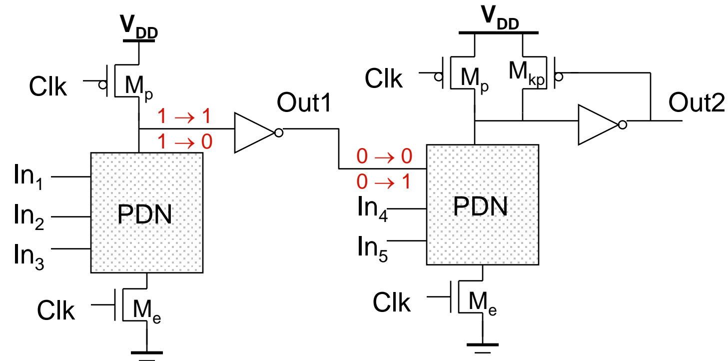
- Like falling dominoes.




**CLK=0: Precharge**
**CLK=1: Logic propagates thru series of gates like dominoes falling.**

# Domino Logic with Keeper at output

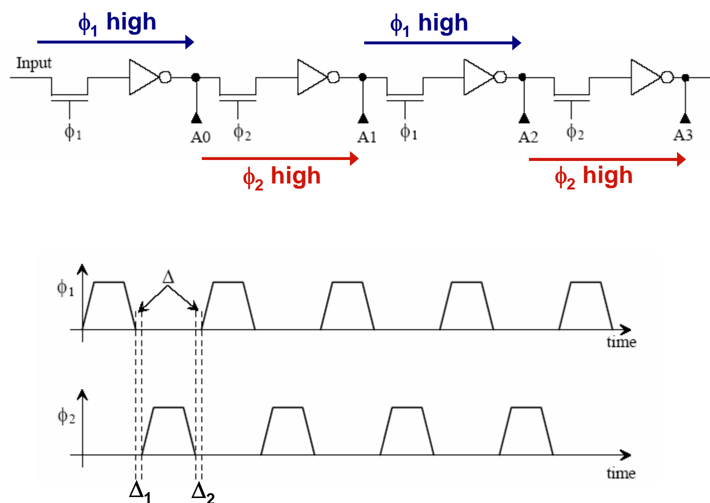
- Use small $M_{kp}$



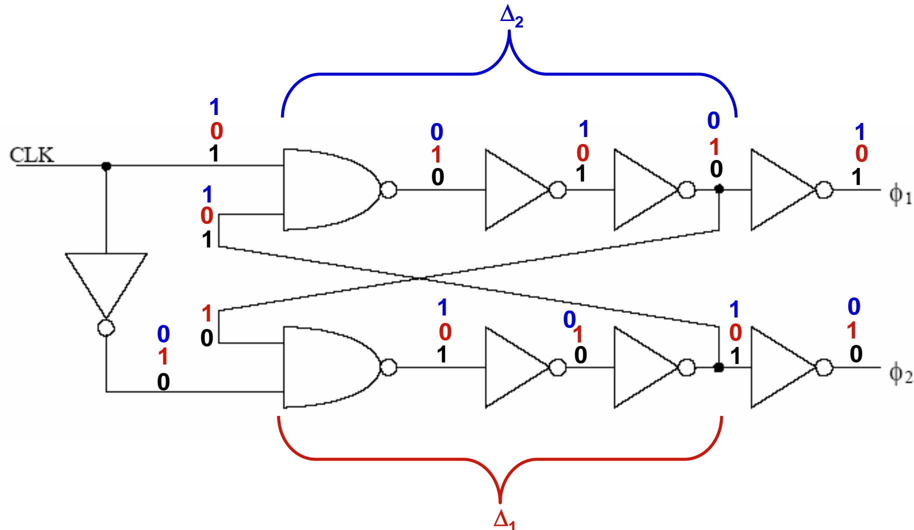



# Dynamic Shift Register

- Non-overlapping clock



# Non-Overlapping CLK

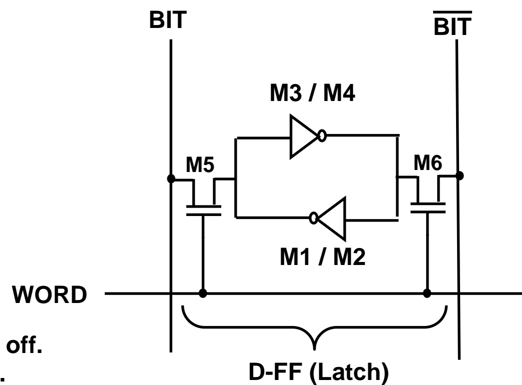



Initially, CLK=1 (Black). $\phi_1$ =1 & $\phi_2$ =0.
CLK ➔ 0 (Red)
CLK ➔ 1 (Blue)



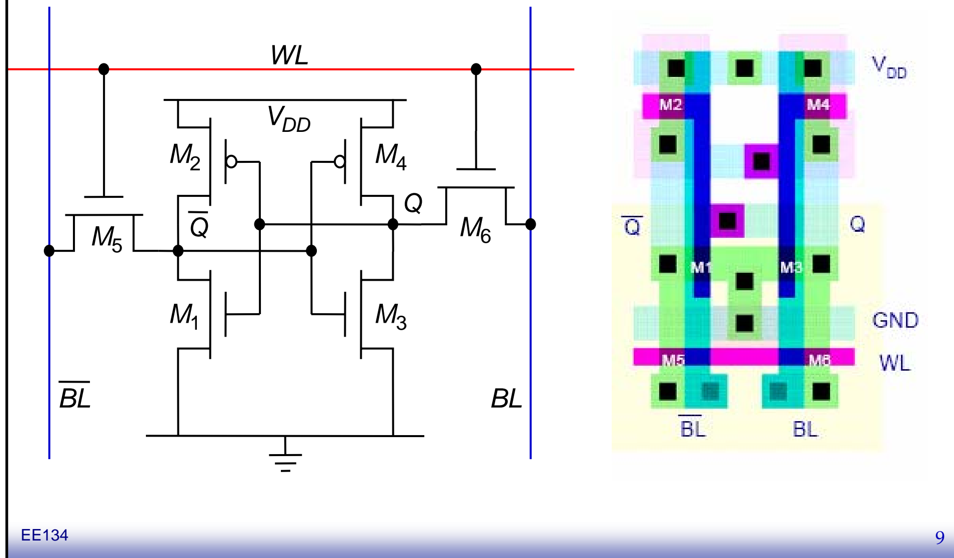
# Static RAM (SRAM)

## ❑ SRAM Cell: Simple D-FF (Latch)




- Word line low
  - Pass transistors M5 and M6 off.
  - Data latched in inverter pair.
- Word line high: Writing / Reading
  - Writing: Write by force.
  - Reading: BIT and $\overline{BIT}$ precharged to either $V_{DD}$ or $V_{DD}/2$. Read.

# SRAM at transistor level






# EE134 Summary

- Major Challenges
  - Cost
  - Power Consumption
  - Robustness
  - Complexity

- Some new circuit solutions and design methodologies are coming.

# Technology Scaling

| | 2004 | 2006 | 2008 | 2010 | 2012 | 2014 | 2016 | 2018 |
|---|---|---|---|---|---|---|---|---|
| Technology Node (nm) | 90 | 65 | 45 | 32 | 22 | 16 | 11 | 8 |
| Integration Capacity (BT) | 0.5 | 1 | 2 | 4 | 8 | 16 | 32 | 64 |
| Delay = CV/I scaling | 0.7 | ~0.7 | >0.7 | Delay scaling will slow down | | | | |
| Energy/Logic Op scaling | >0.35 | >0.5 | >0.5 | Energy scaling will slow down | | | | |
| Bulk Planar CMOS | High Probability | | | | Low Probability | | | |
| Alternate, 3G etc | Low Probability | | | | High Probability | | | |
| Variability | Medium | | | High | | Very High | | |
| ILD (K) | ~3 | <3 | Reduce slowly towards 2-2.5 | | | | | |
| RC Delay | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Metal Layers | 6-7 | 7-8 | 8-9 | 0.5 to 1 layer per generation | | | | |

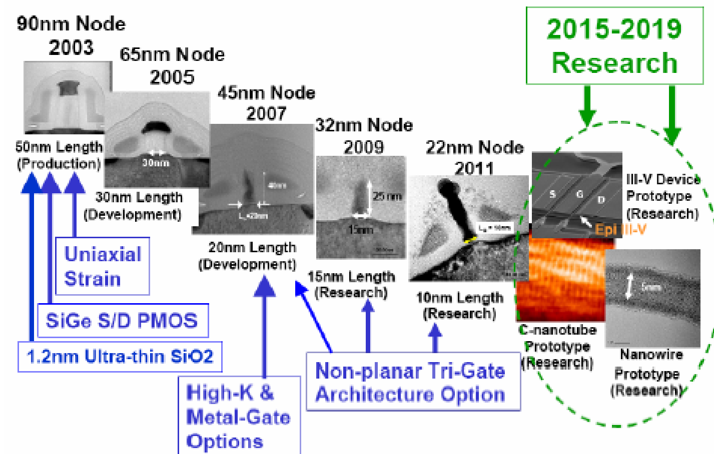
*Courtesy: R. Krishnamurthy (Intel)*

Internal University FCRP(MARCO)

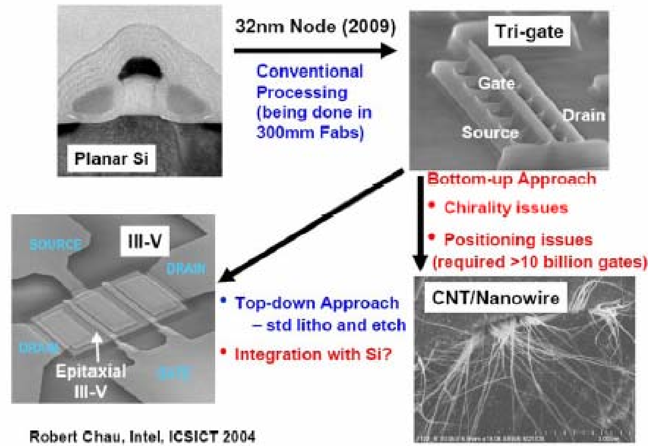
SRC



# Research Roadmap

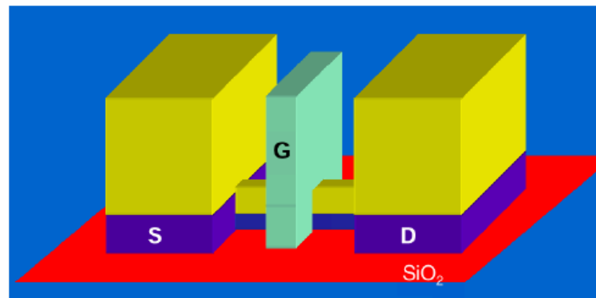


# Device Evolution






# 25 nm FinFET



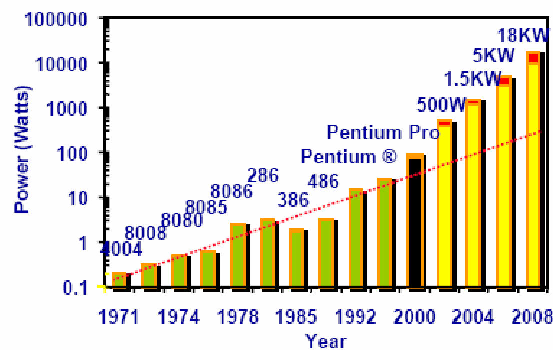

25 nm MOS transistor (Folded Channel)

# Cost

- Mask cost in 90nm technology is over $1M.
- Bugs are very expensive.
- Design effort increases in DSM.
- Cost of new tools.
- Non-recurring costs dominate the price effectiveness of low-volume ASICs.
- Need to have a product that can fit multiple applications, customers (flexibility).



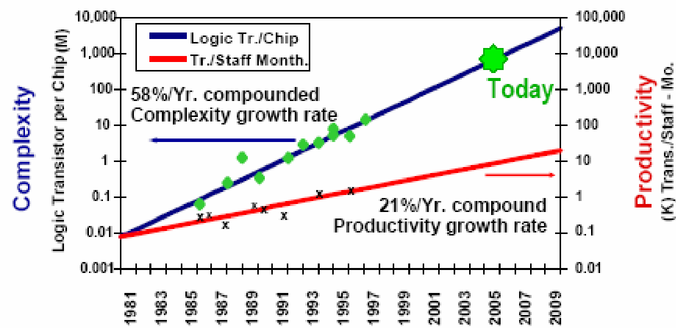
# Power has become a Problem




Source: S. Borkar (Intel)

Power delivery and dissipation will be prohibitive

# The Productivity Gap




*Source: Sematech*

**Complexity outpaces design productivity**



# Challenges in Digital Design

## ❑ The Deep Submicron (DSM) Effect

### ∝ DSM

**"Microscopic Problems"**

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

**Everything Looks a Little Different**

### ∝ 1/DSM

**"Macroscopic Issues"**

- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

**…and There's a Lot of Them!**

# ABET Evaluation: Course Objectives

- Things that you should have learned in EE134.

| | Course Objective | Very Poorly | | | | Very Well |
|---|---|---|---|---|---|---|
| 1 | Understand the device model for a modern short-channel FET. | 1 | 2 | 3 | 4 | 5 |
| 2 | Understand the parasitic diodes and capacitors of an inverter. | 1 | 2 | 3 | 4 | 5 |
| 3 | Ability to layout, DRC, and LVS a CMOS digital IC. | 1 | 2 | 3 | 4 | 5 |
| 4 | Calcuate delay times through inverters and logic gates. | 1 | 2 | 3 | 4 | 5 |
| 5 | Size a chain of inverters to drive a large capacitive load. | 1 | 2 | 3 | 4 | 5 |
| 6 | Design static CMOS logic gates. | 1 | 2 | 3 | 4 | 5 |
| 7 | Understand  CMOS transmisison gates. | 1 | 2 | 3 | 4 | 5 |
| 8 | Understand CMOS transmission gate latches and registers. | 1 | 2 | 3 | 4 | 5 |



# ABET: Program Outcomes

| | Attribute | Very Poorly | | | | Very Well |
|---|---|---|---|---|---|---|
| **a** | An ability to apply knowledge of mathematics, science, and engineering | 1 | 2 | 3 | 4 | 5 |
| **b** | An ability to design and conduct experiments, as well as to analyze and interpret data | 1 | 2 | 3 | 4 | 5 |
| **c** | An ability to design a system, component, or process to meet desired needs | 1 | 2 | 3 | 4 | 5 |
| **d** | An ability to function on multi-disciplinary teams | 1 | 2 | 3 | 4 | 5 |
| **e** | An ability to identify, formulate, and solve engineering problems | 1 | 2 | 3 | 4 | 5 |
| **f** | An understanding of professional ethical responsibility | 1 | 2 | 3 | 4 | 5 |
| **g** | An ability to communicate effectively | 1 | 2 | 3 | 4 | 5 |
| **h** | The broad education necessary to understand the impact of engineering solutions in a global and societal context | 1 | 2 | 3 | 4 | 5 |
| **i** | A recognition of the need for, and an ability to engage in life-long learning | 1 | 2 | 3 | 4 | 5 |
| **j** | A knowledge of contemporary issues | 1 | 2 | 3 | 4 | 5 |
| **k** | An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice | 1 | 2 | 3 | 4 | 5 |

"That's all Folks!"