Digital Integrated Circuit (IC) Layout and Design - Week 4, Lecture 7

- http://www.ee.ucr.edu/~rlake/EE134.html

Reading

- Week 1 - Read Chapter 1 of text.
- Week 2 - Read Chapter 2 of text.
- Week 3 - Read Chapter 3 of text.
- Week 4 - Read Chapter 5 of text.

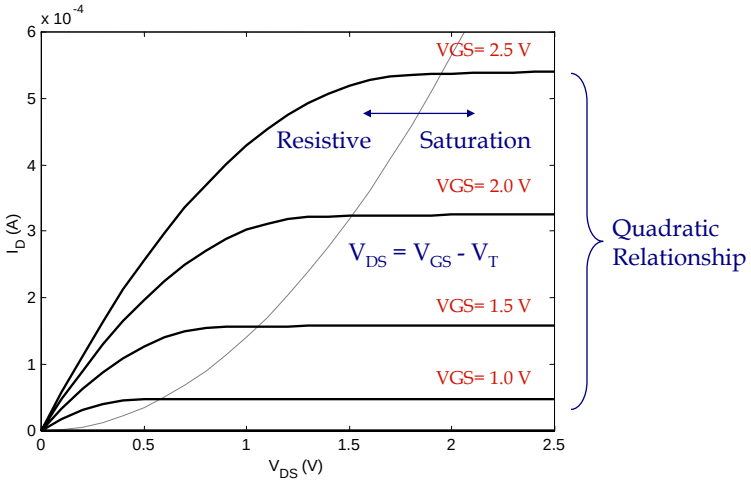
Review

- MOS Transistor (Ch. 3)
  - Modes of Operation
  - Deep sub-micron MOS
  - Latch-up (finish up)

New

- Inverter (Ch. 5)
  - Voltage transfer curve (VTC)
  - Switching Point

Current-Voltage Relations
A good ol' Transistor



Modes of Operation (Good ol' Transistor)

- **Cutoff:**

  $V_{GS} < V_T$ $\quad\quad$ $I_D = 0$

- **Resistive or Linear:**

  $V_{DS} < V_{GS} - V_T$ & $V_{GS} > V_T$

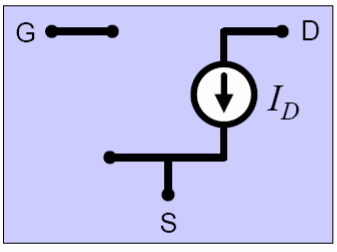
$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- **Saturation**

  $V_{DS} > V_{GS} - V_T$
  $V_{GS} > V_T$

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

A Model for Manual Analysis



$V_{DS} > V_{GS} - V_T$ **Saturation:**

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$

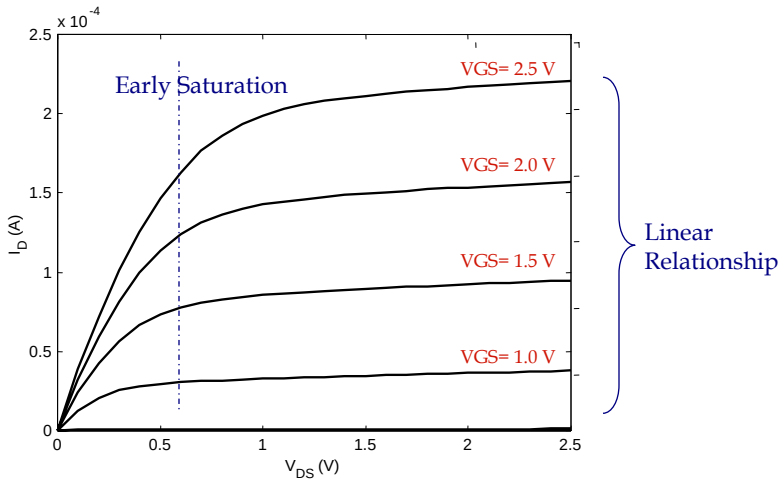
$V_{DS} < V_{GS} - V_T$ **Resistive:**

$$I_D = k_n' \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

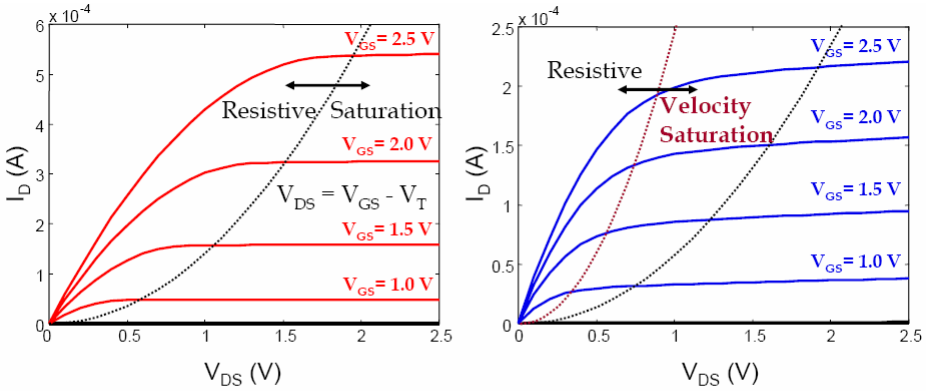
with

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

Current-Voltage Relations
The Deep-Submicron Era



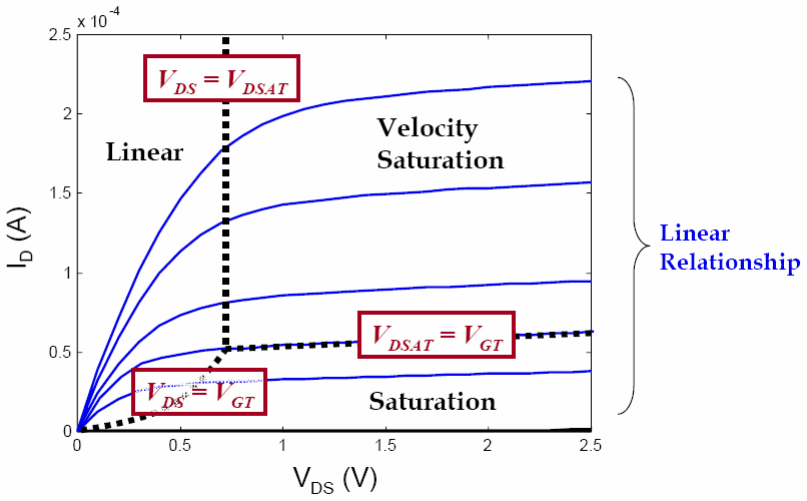
I_D versus V_{DS}



Long Channel (L=10μm) W/L=1.5 Short Channel (L=0.25μm)

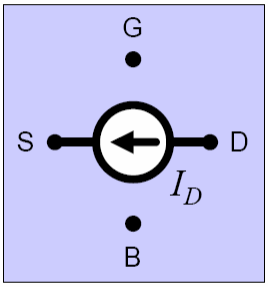
Regions of Operation - Simplified

- Define $V_{GT} = V_{GS} - V_T$ $\quad V_{DSAT} \approx L \cdot \xi_c$



A Unified Model for Manual Analysis

define $V_{GT} = V_{GS} - V_T$



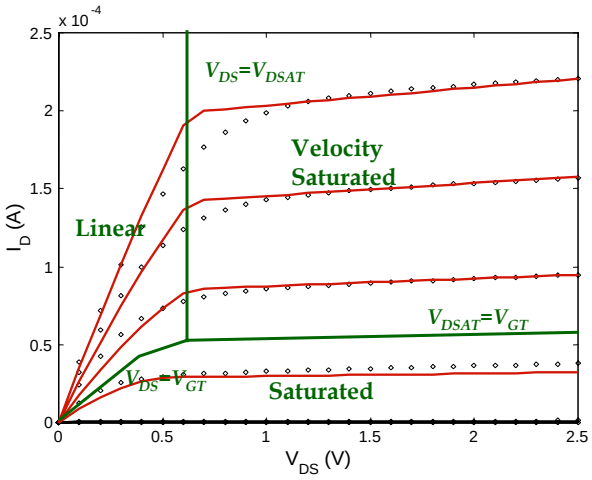
for $V_{GT} \leq 0$: $I_D = 0$

for $V_{GT} \geq 0$:

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{\min} - \frac{V_{\min}^2}{2} \right) \cdot \left(1 + \lambda \cdot V_{DS}\right)$$

with $V_{min} = \min (V_{GT}, V_{DS}, V_{DSAT})$

Simple Model versus SPICE



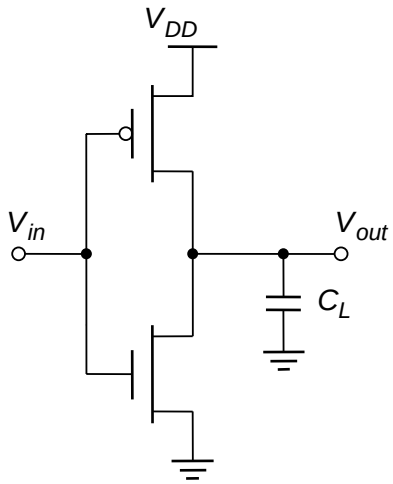
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

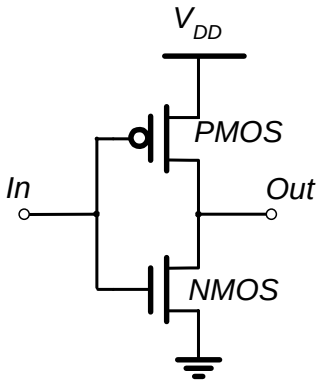
	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

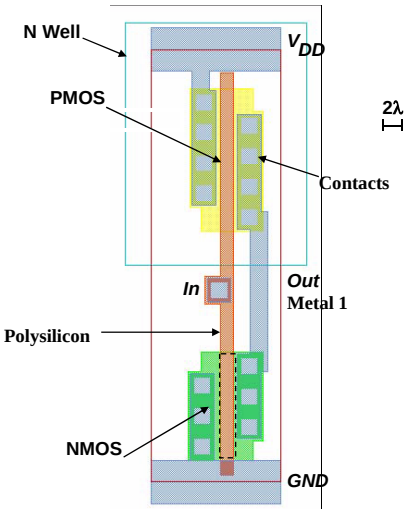
I keep all signs positive for PMOS and use V_{SG}, V_{SD}, I_{SD}.

Ch. 5
The CMOS Inverter: A First Glance



CMOS Inverter

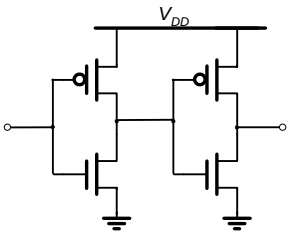


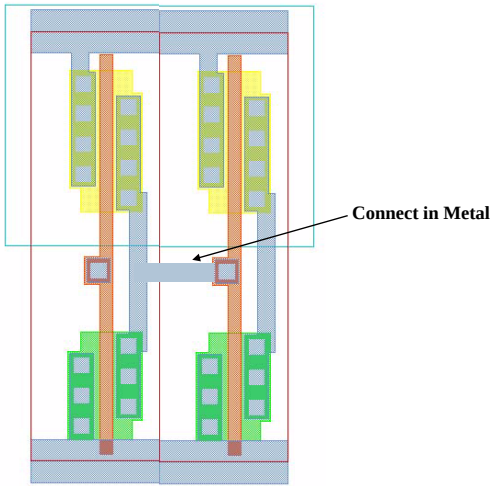


Two Inverters

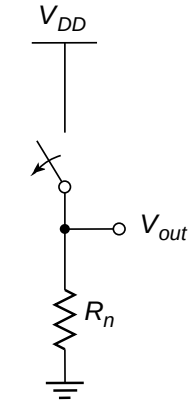
Share power and ground

Abut cells

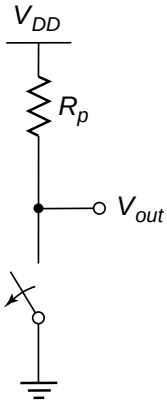




CMOS Inverter
First-Order DC Analysis



$V_{in} = V_{DD}$



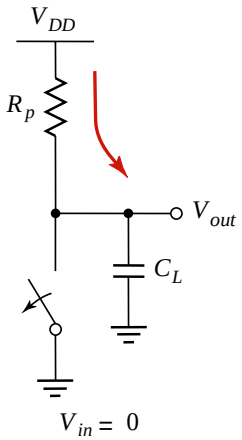
$V_{in} = 0$

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

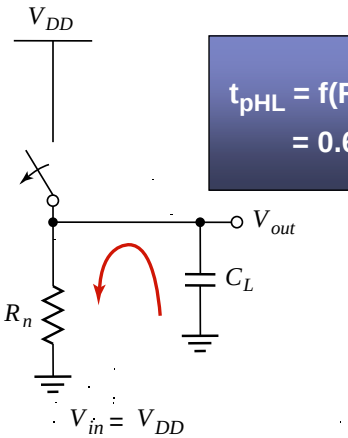
CMOS Inverter Properties

- Full rail-to-rail voltage swing
  - $V_{OH} = V_{DD}$ & $V_{OL} = 0$
- Logic levels independent of transistor size
  - "Ratioless" logic
- Low output resistance (kΩ range)
- High input resistance
- No direct current path in steady state (ignoring leakage)

CMOS Inverter: Transient Response



(a) Low-to-high

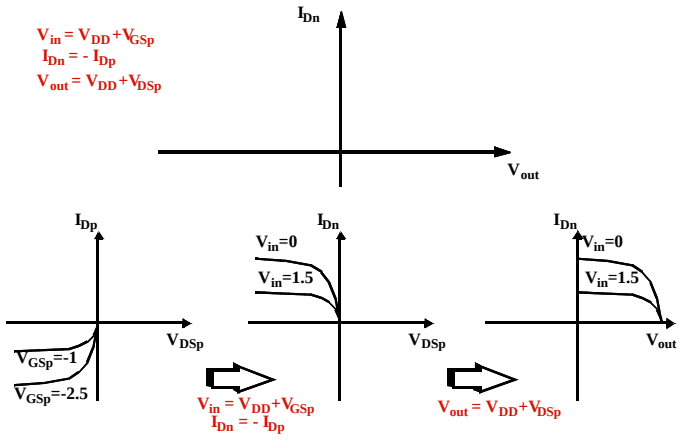


(b) High-to-low

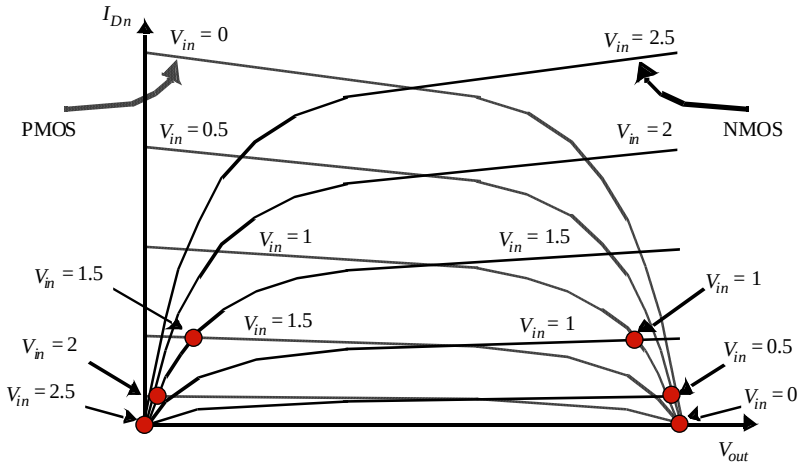
$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_n\ C_L$

Voltage Transfer Characteristic

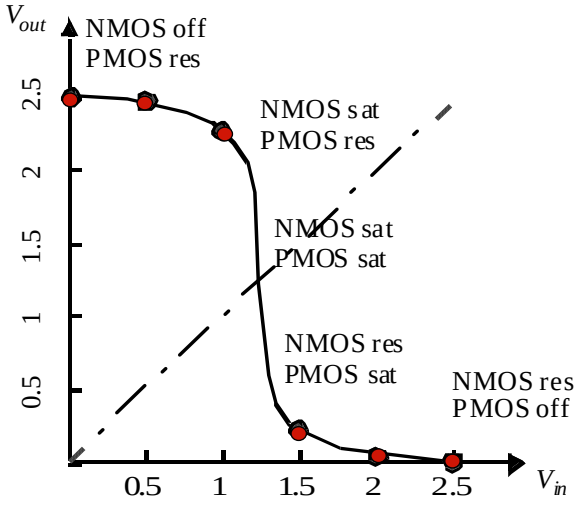
PMOS Load Lines



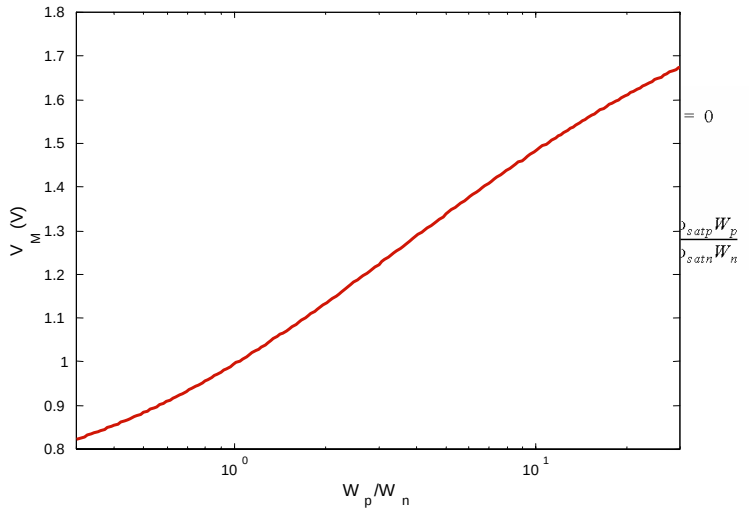
CMOS Inverter Load Characteristics



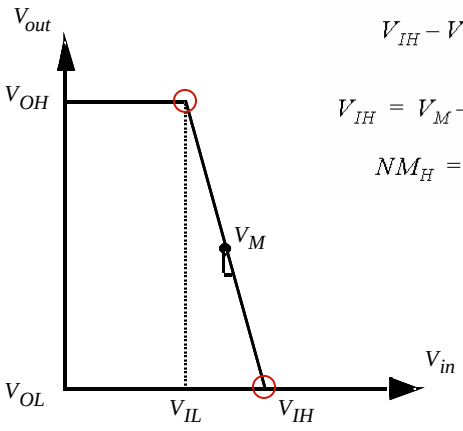
CMOS Inverter VTC



Switching Threshold as a function of Transistor Ratio



Determining V_{IH} and V_{IL}

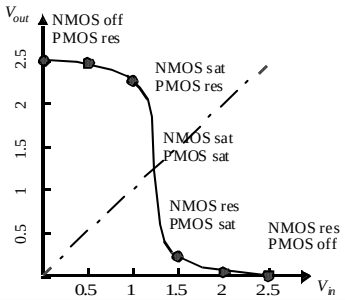


$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

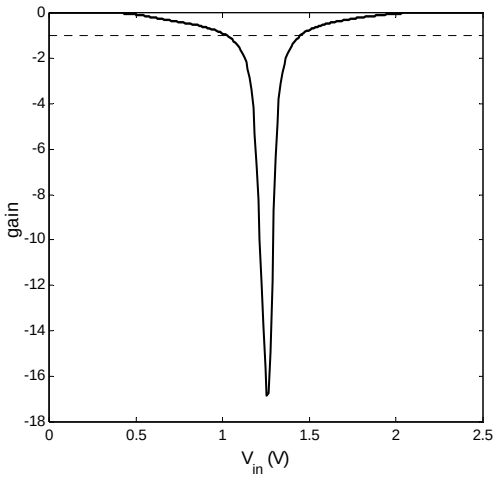
$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

A simplified approach

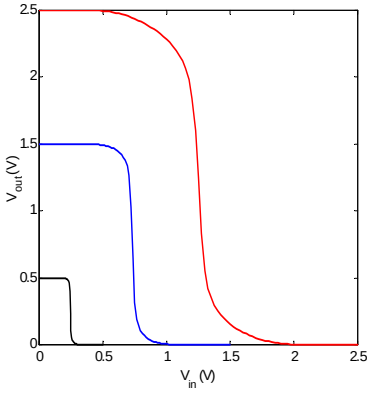


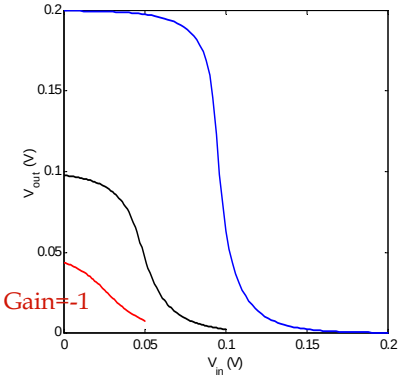
Inverter Gain



$$g = -\frac{1}{I_D(V_M)}\frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p}$$
$$\approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

Gain as a function of VDD





Impact of Process Variations