

## Digital Integrated Circuit (IC) Layout and Design - Week 4, Lecture 7

- <http://www.ee.ucr.edu/~rlake/EE134.html>

## Reading

- Week 1 - Read Chapter 1 of text.
- Week 2 - Read Chapter 2 of text.
- Week 3 - Read Chapter 3 of text.
- Week 4 - Read Chapter 5 of text.

## Review

### □ MOS Transistor (Ch. 3)

- Modes of Operation
- Deep sub-micron MOS
- Latch-up (finish up)

## New

### □ Inverter (Ch. 5)

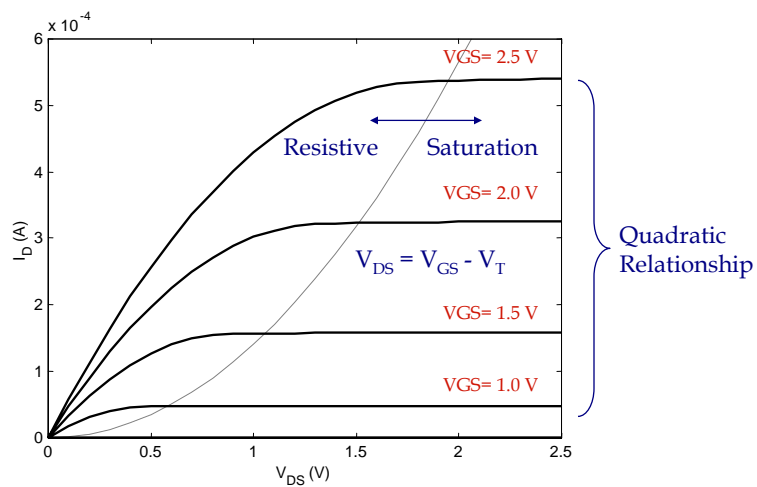
- Voltage transfer curve (VTC)
- Switching Point



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## Current-Voltage Relations A good ol' Transistor



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## Modes of Operation (Good ol' Transistor)

□ **Cutoff:**

$$V_{GS} < V_T$$

$$I_D = 0$$

□ **Resistive or Linear:**

$$V_{DS} < V_{GS} - V_T \text{ \& } V_{GS} > V_T$$

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

□ **Saturation**

$$V_{DS} > V_{GS} - V_T \text{ \& } V_{GS} > V_T$$

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

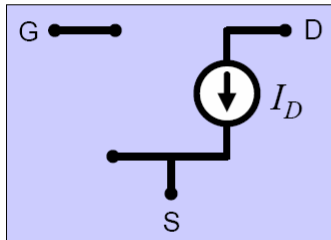
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## A Model for Manual Analysis

$V_{DS} > V_{GS} - V_T$  **Saturation:**

$$I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$



$V_{DS} < V_{GS} - V_T$  **Resistive:**

$$I_D = k'_n \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

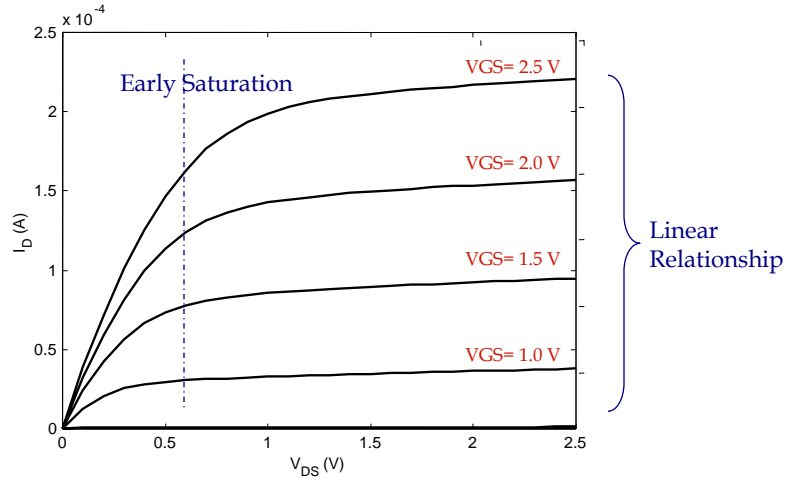
with

$$V_T = V_{T0} + \gamma \cdot \left( \sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

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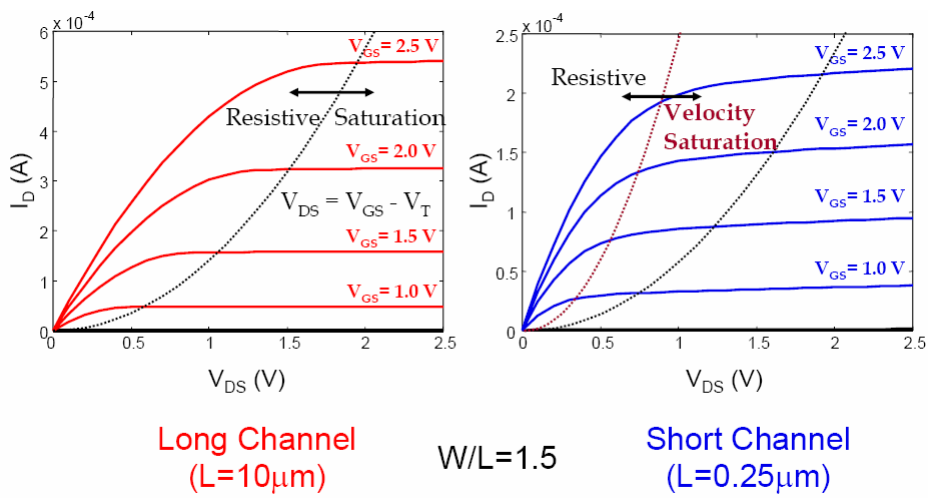
## Current-Voltage Relations The Deep-Submicron Era



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## $I_D$ versus $V_{DS}$

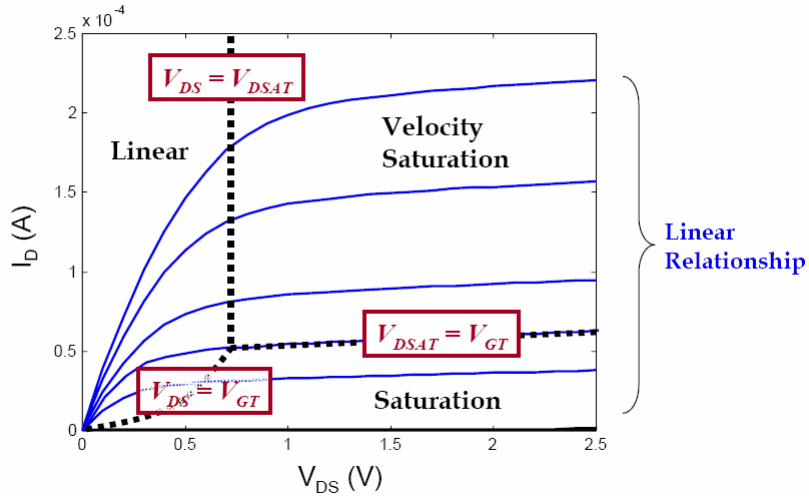


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## Regions of Operation - Simplified

◆ Define  $V_{GT} = V_{GS} - V_T$        $V_{DSAT} \approx L \cdot \xi_c$



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## A Unified Model for Manual Analysis

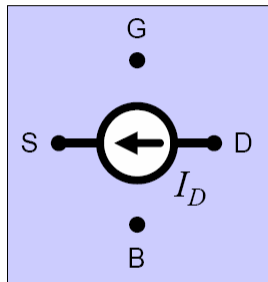
define  $V_{GT} = V_{GS} - V_T$

for  $V_{GT} \leq 0$ :  $I_D = 0$

for  $V_{GT} \geq 0$ :

$$I_D = k' \cdot \frac{W}{L} \cdot \left( V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

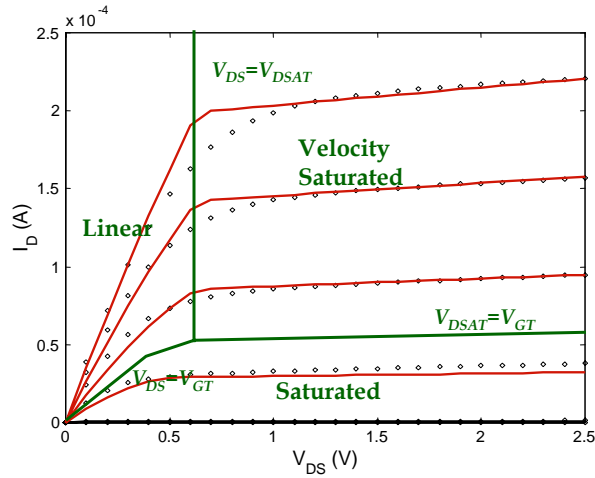
with  $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$



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## Simple Model versus SPICE



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## Transistor Model for Manual Analysis

**Table 3.2** Parameters for manual model of generic 0.25  $\mu\text{m}$  CMOS process (minimum length device).

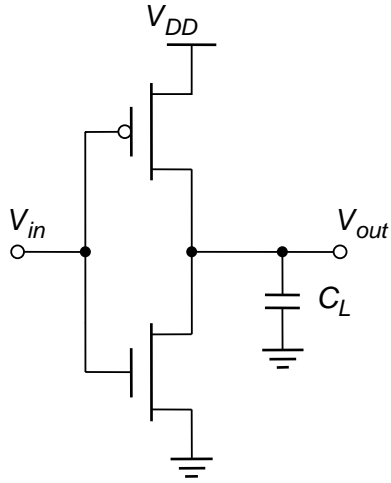
	$V_{T0}$ (V)	$\gamma$ ( $\text{V}^{0.5}$ )	$V_{DSAT}$ (V)	$K'$ ( $\text{A}/\text{V}^2$ )	$\lambda$ ( $\text{V}^{-1}$ )
NMOS	0.43	0.4	0.63	$115 \times 10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30 \times 10^{-6}$	-0.1

**I keep all signs positive for PMOS and use  $V_{SG}$ ,  $V_{SD}$ ,  $I_{SD}$ .**

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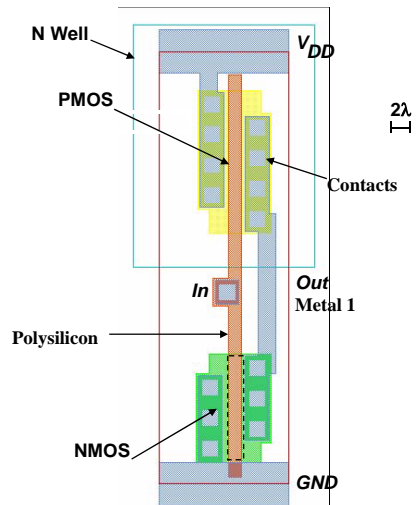
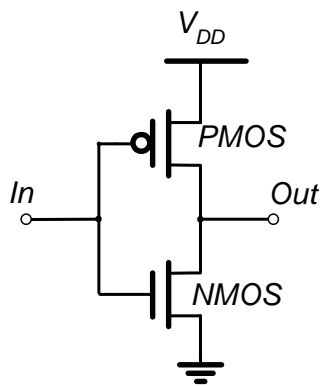
# Ch. 5 The CMOS Inverter: A First Glance



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# CMOS Inverter



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## Two Inverters

Share power and ground

Abut cells

The diagram shows two inverters connected in series. The first inverter's output is connected to the second inverter's input. The circuit is powered by  $V_{DD}$  and ground. To the right, a cross-sectional view of the two inverters is shown, illustrating how they share power and ground connections through metal layers. A label 'Connect in Metal' points to the shared metal connections between the two cells.

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## CMOS Inverter

### First-Order DC Analysis

The analysis shows two states of a CMOS inverter. In the first state, the input  $V_{in} = V_{DD}$  is high, and the output  $V_{out}$  is pulled down to ground through a resistor  $R_n$ . In the second state, the input  $V_{in} = 0$  is low, and the output  $V_{out}$  is pulled up to  $V_{DD}$  through a resistor  $R_p$ .

$$V_{OL} = 0$$

$$V_{OH} = V_{DD}$$

$$V_M = f(R_n, R_p)$$

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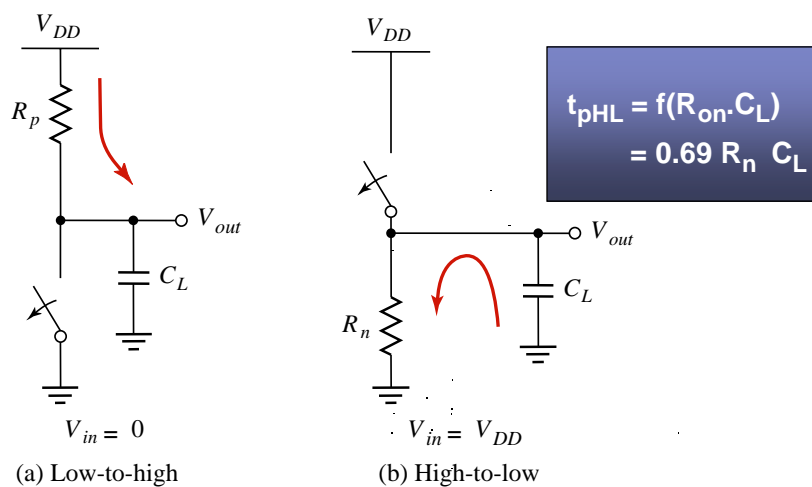
## CMOS Inverter Properties

- Full rail-to-rail voltage swing
  - $V_{OH} = V_{DD}$  &  $V_{OL} = 0$
- Logic levels independent of transistor size
  - “Ratioless” logic
- Low output resistance ( $k\Omega$  range)
- High input resistance
- No direct current path in steady state (ignoring leakage)

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## CMOS Inverter: Transient Response



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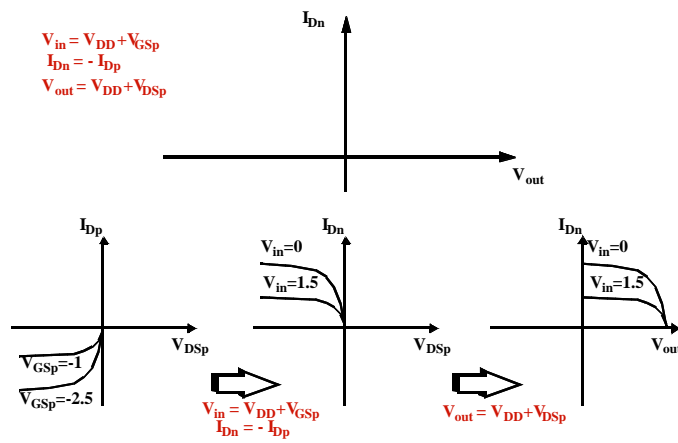
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## Voltage Transfer Characteristic

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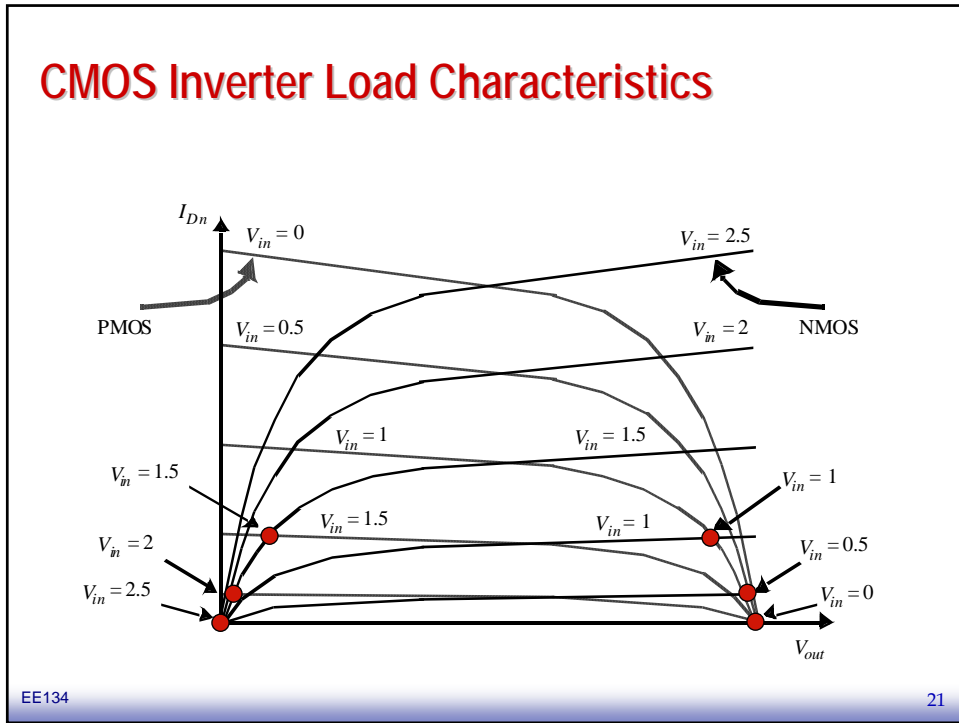
## PMOS Load Lines



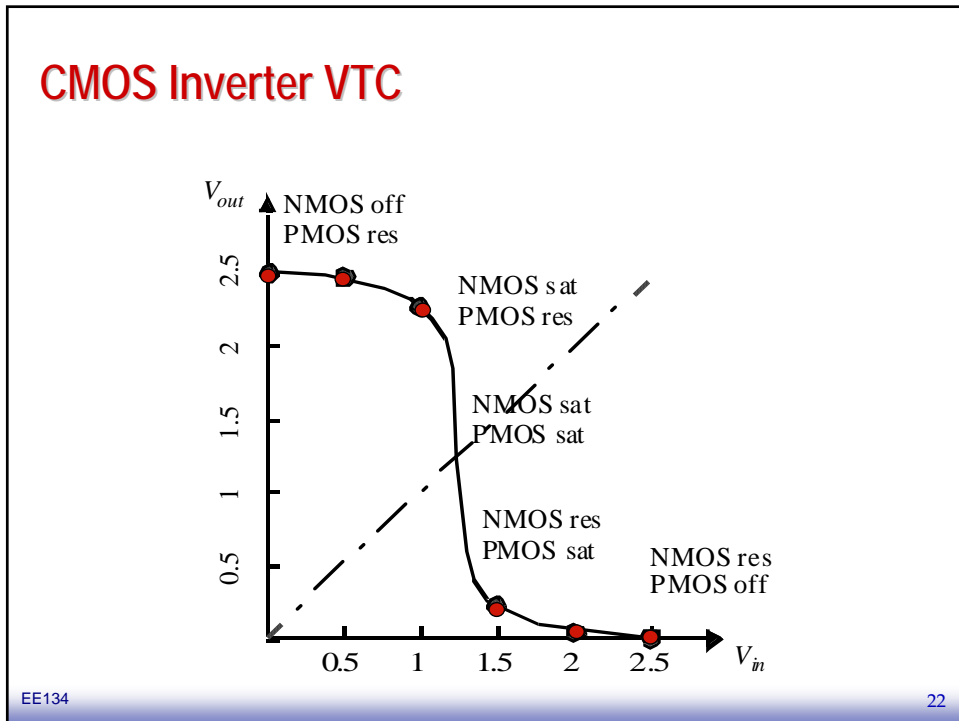
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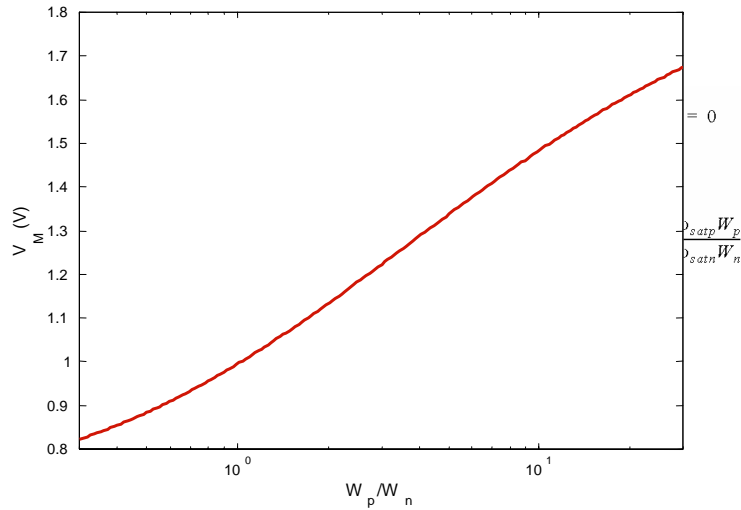
## CMOS Inverter Load Characteristics



## CMOS Inverter VTC



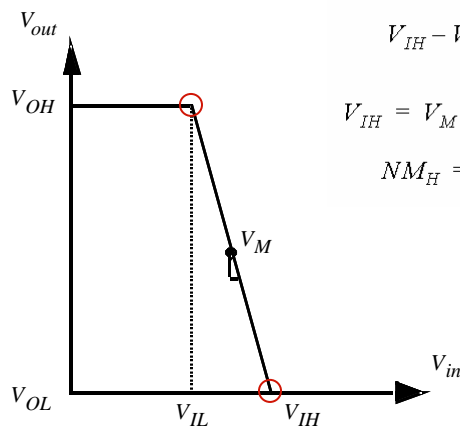
## Switching Threshold as a function of Transistor Ratio



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## Determining $V_{IH}$ and $V_{IL}$

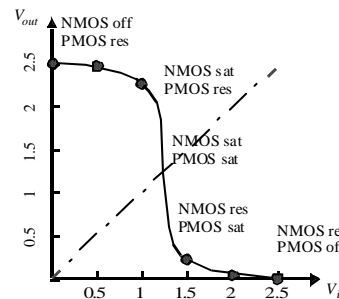


**A simplified approach**

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \quad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

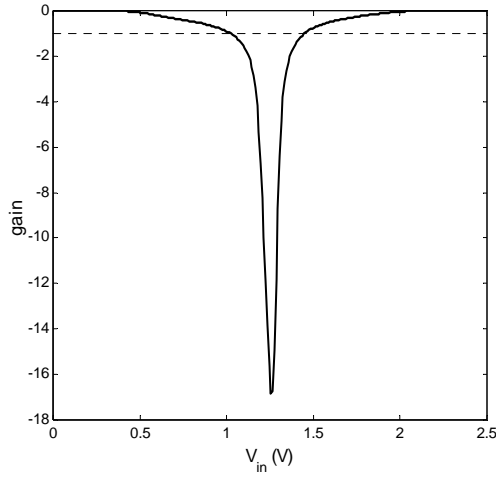
$$NM_H = V_{DD} - V_{IH} \quad NM_L = V_{IL}$$



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## Inverter Gain



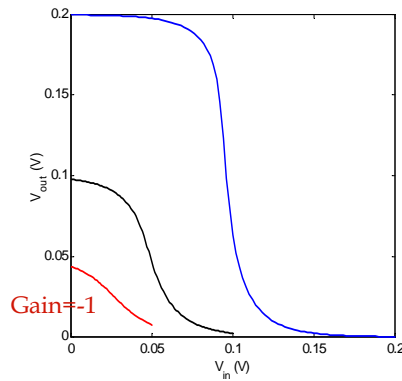
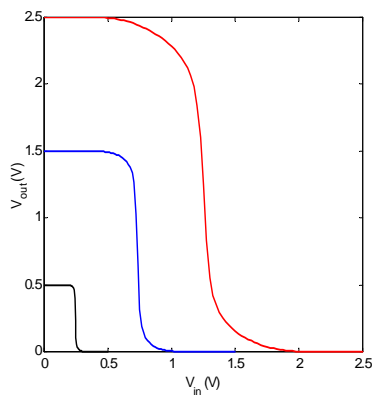
$$g = \frac{1}{I_D(V_M)} \frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p}$$

$$\approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

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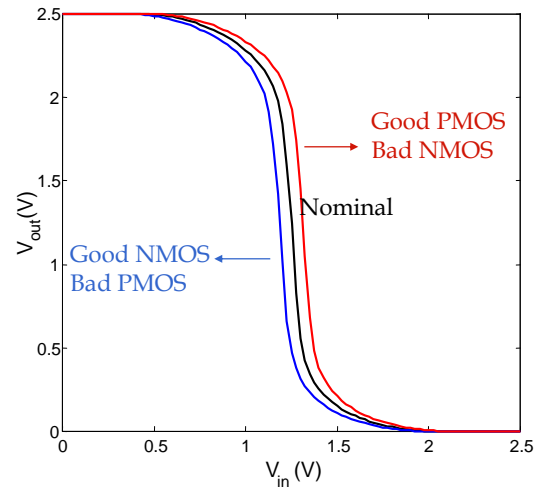
## Gain as a function of VDD



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## Impact of Process Variations



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