Digital Integrated Circuit (IC) Layout and Design - Week 4, Lecture 8

- **http://www.ee.ucr.edu/~rlake/EE134.html**
- **HW 1 due next Tues.**

Reading

- Week 1 - Read Chapter 1 of text.
- Week 2 - Read Chapter 2 of text.
- Week 3 - Read Chapter 3 of text.
- Week 4 - Read Chapter 5 of text.

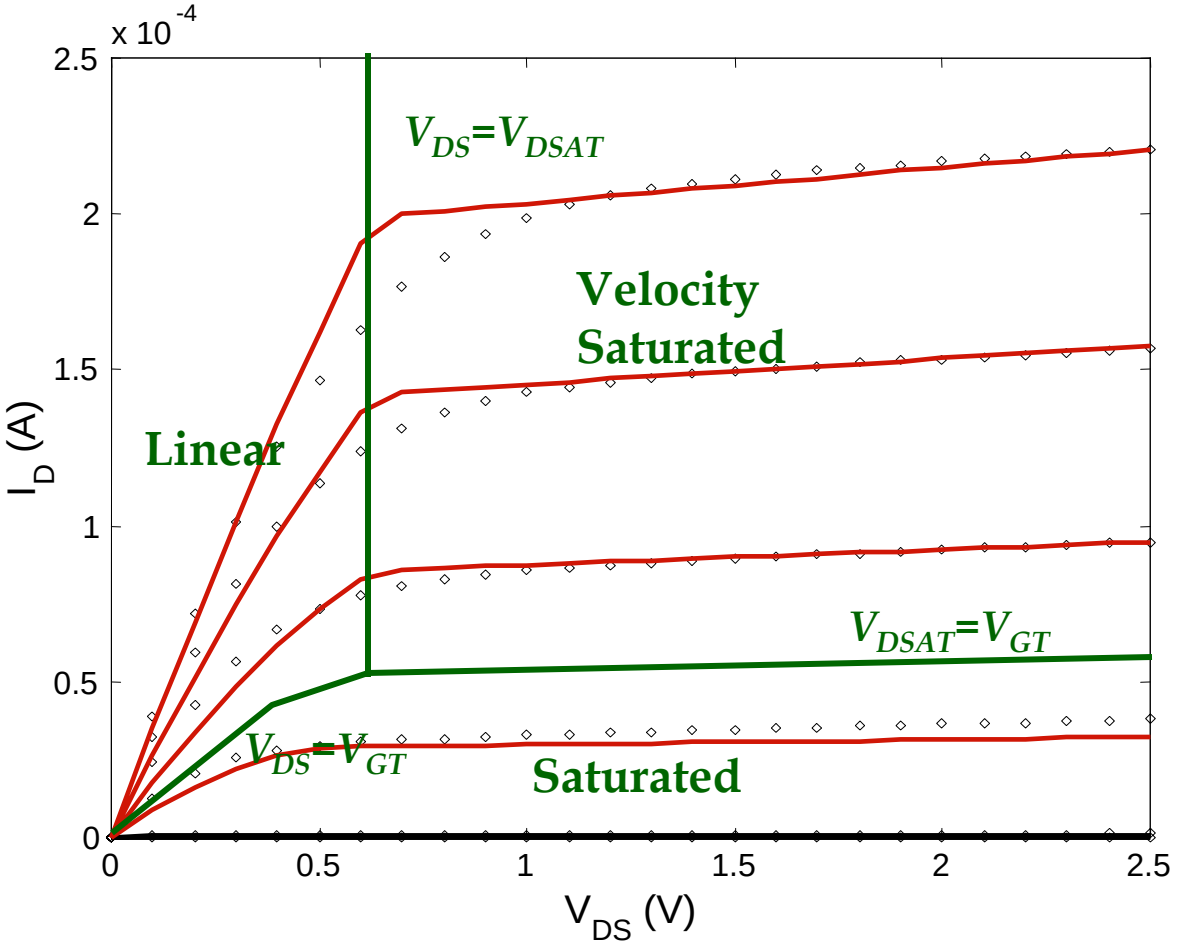
Review/Finish

- **Inverter (Ch. 5)**
  - Voltage transfer curve (VTC)
  - Switching Point

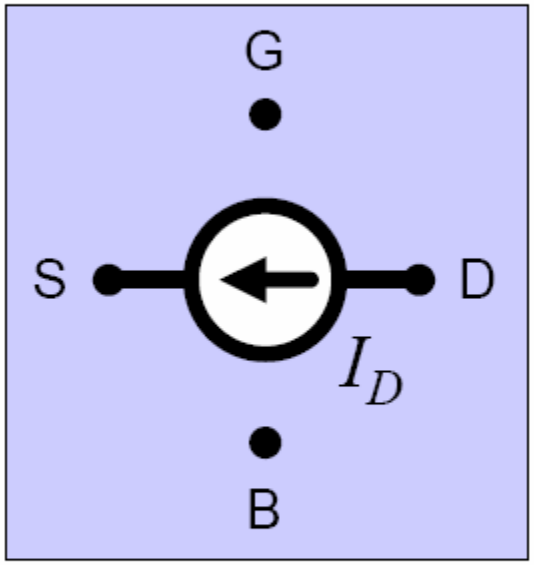
New

- **Inverter (Ch. 5)**
  - Capacitance
  - Switching delay time

Simple Model versus SPICE



A Unified Model for Manual Analysis



define $V_{GT} = V_{GS} - V_T$

for $V_{GT} \leq 0$: $I_D = 0$

for $V_{GT} \geq 0$:

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{\min} - \frac{V_{\min}^2}{2} \right) \cdot \left(1 + \lambda \cdot V_{DS}\right)$$

with $V_{min} = \min\left(V_{GT}, V_{DS}, V_{DSAT}\right)$

Transistor Model for Manual Analysis

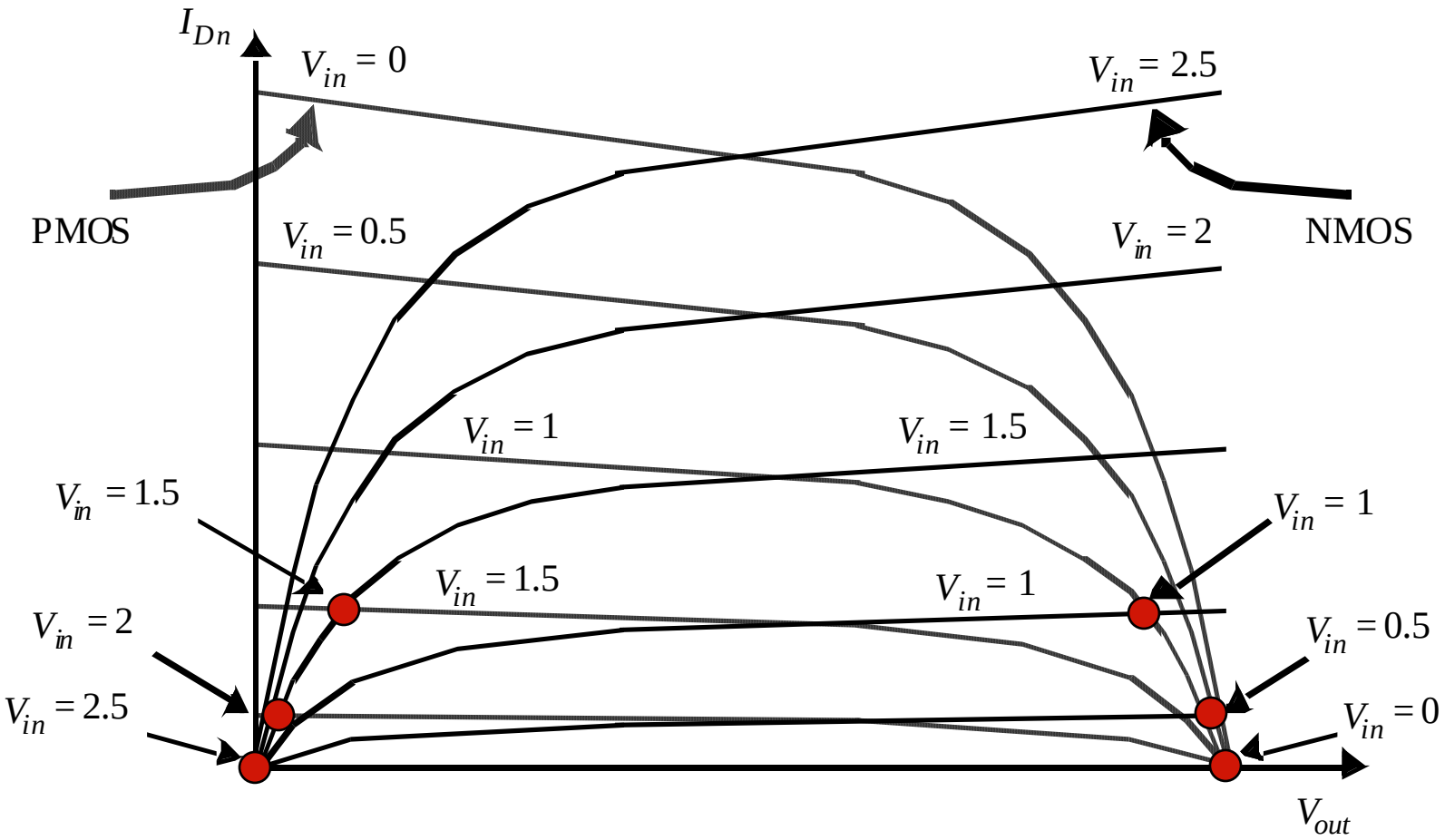
Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	K' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

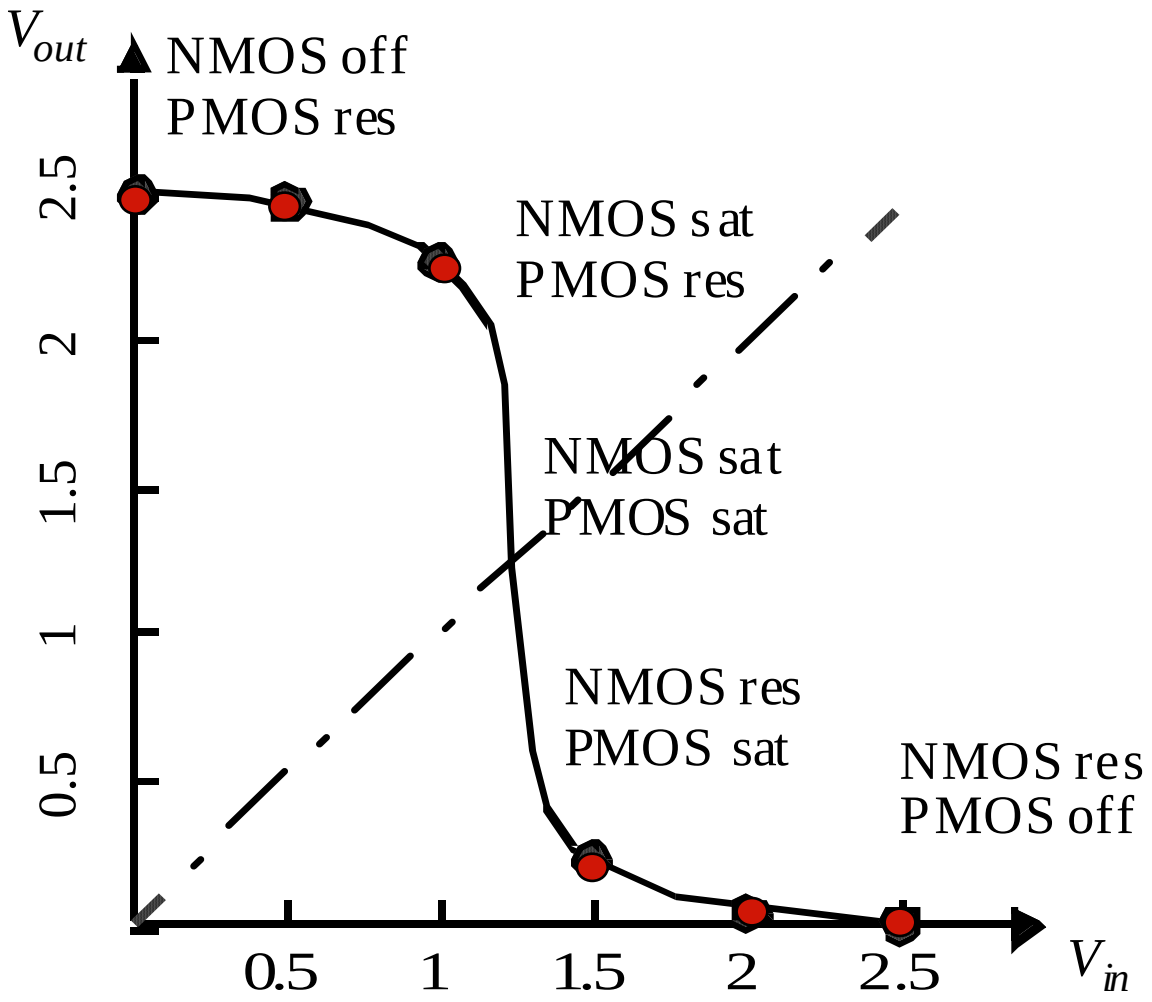
I keep all signs positive for PMOS and use V_{SG}, V_{SD}, I_{SD}.

Voltage Transfer Characteristic

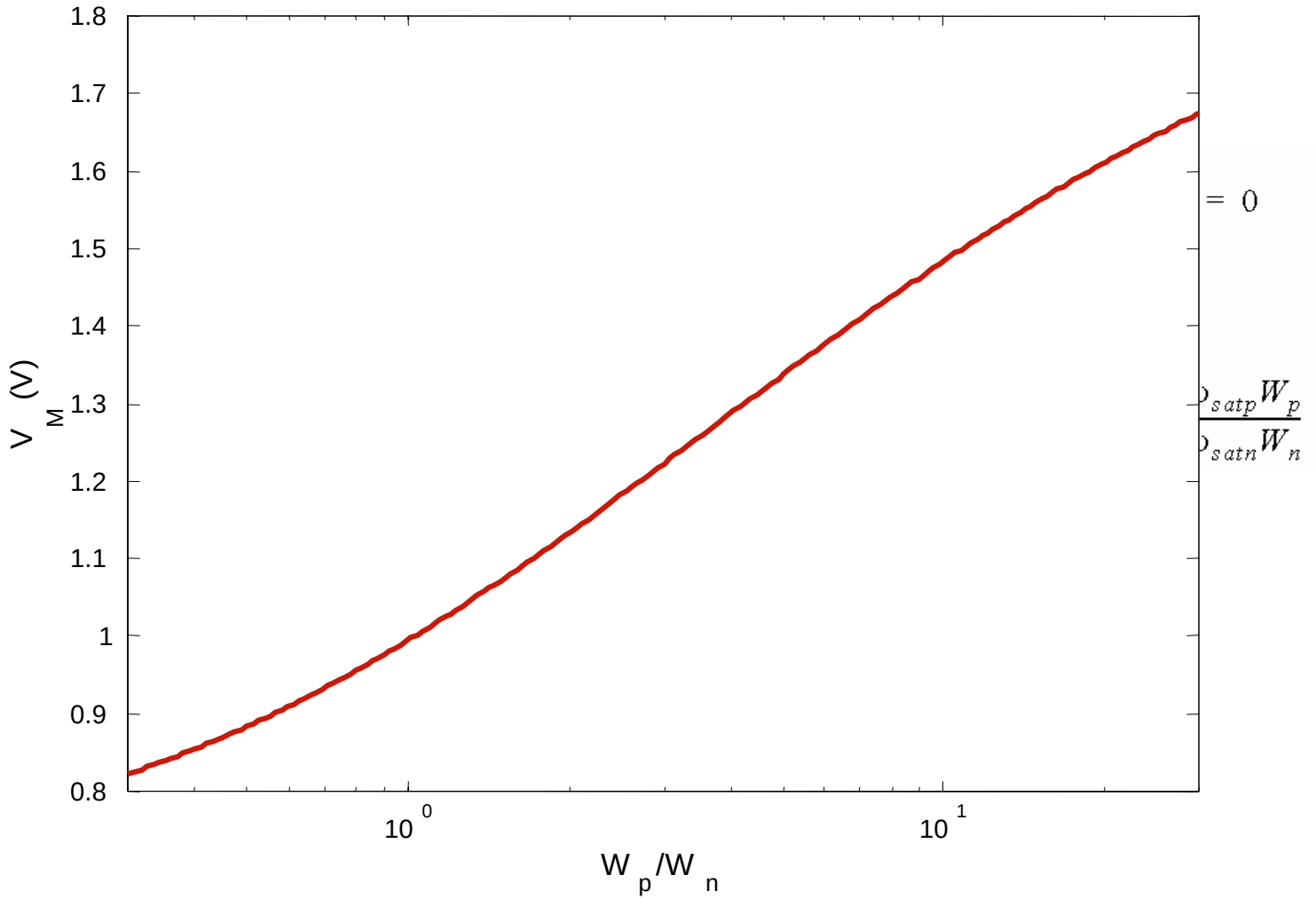
CMOS Inverter Load Characteristics



CMOS Inverter VTC



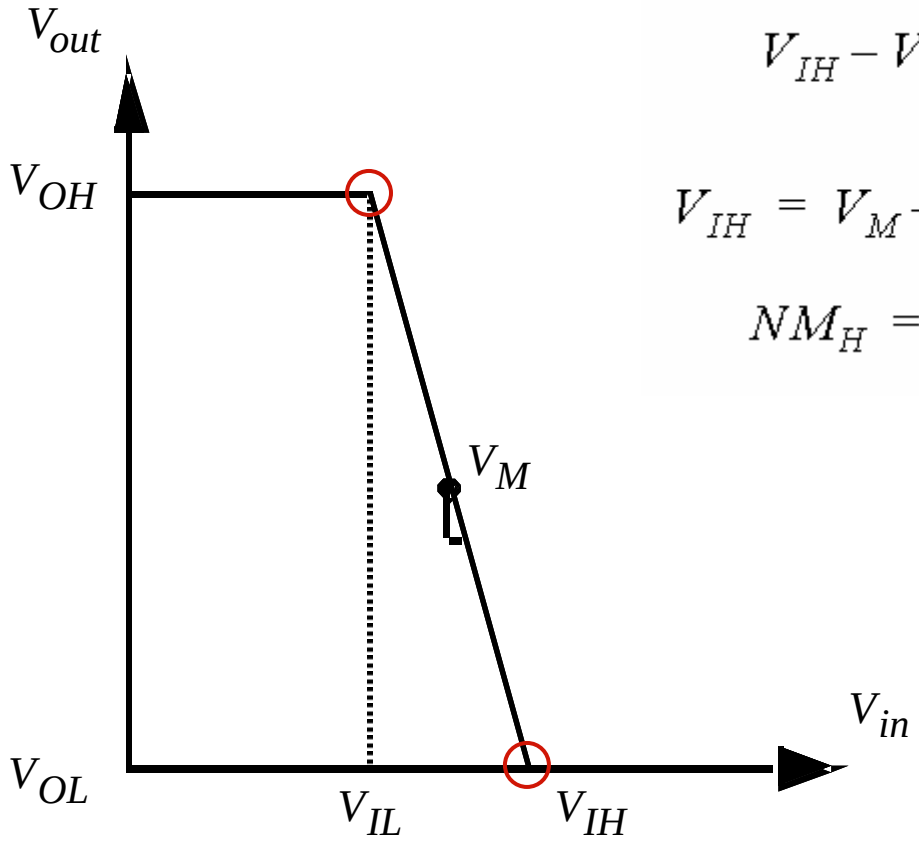
Switching Threshold as a function of Transistor Ratio



$= 0$

$\frac{\mu_{satp} W_p}{\mu_{satn} W_n}$

Determining V_{IH} and V_{IL}

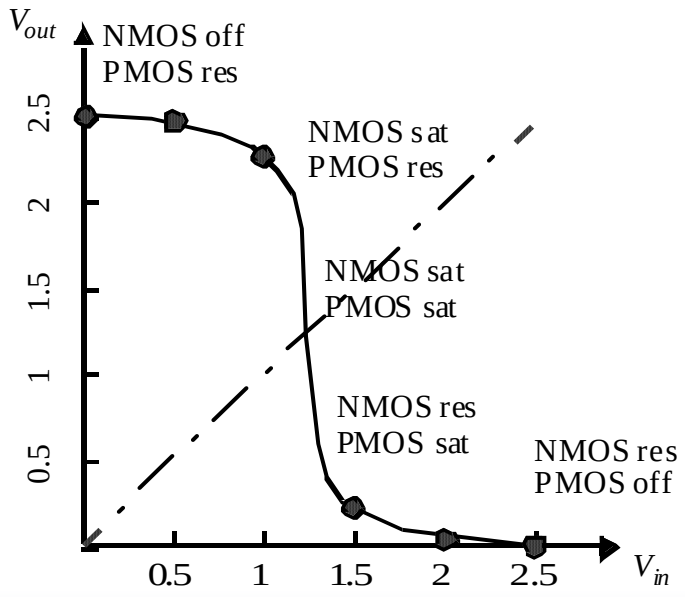


$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

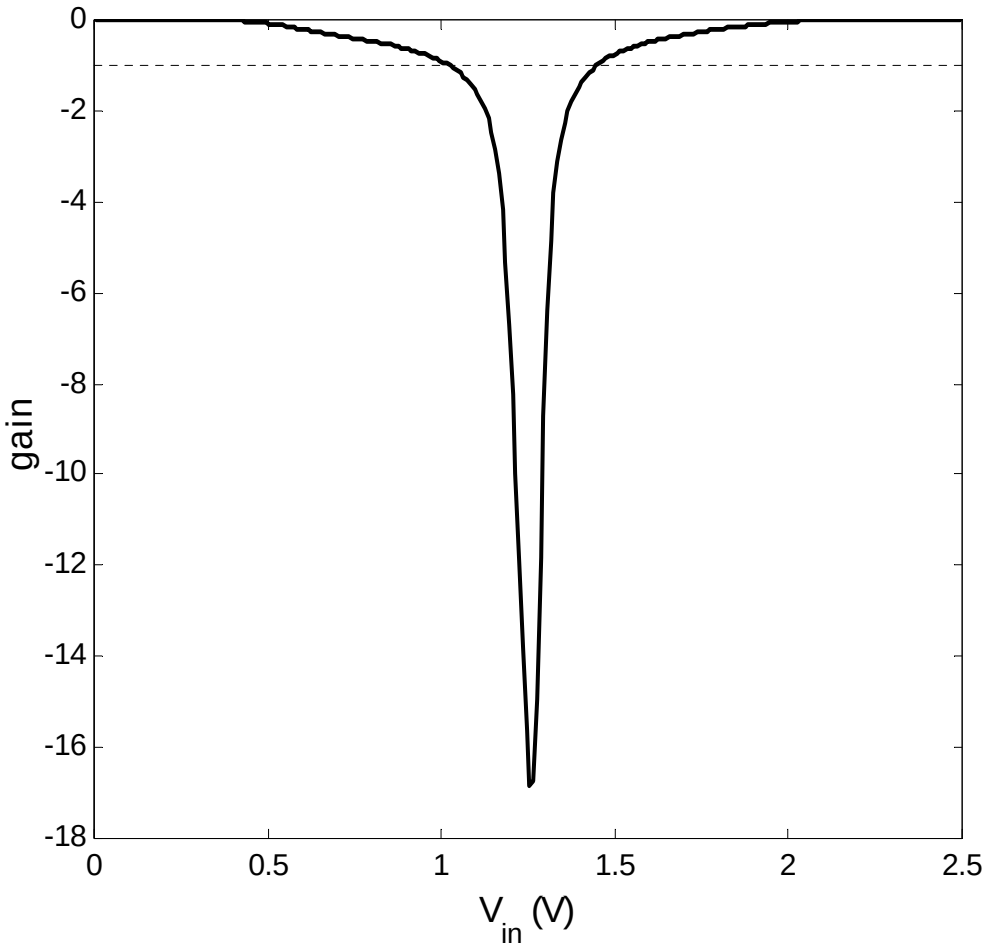
$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

A simplified approach



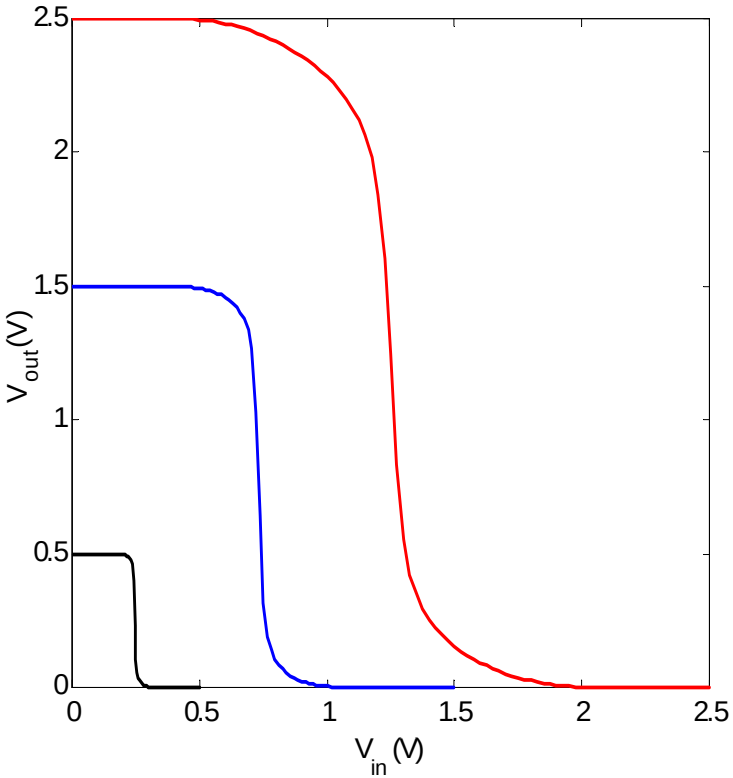
Inverter Gain

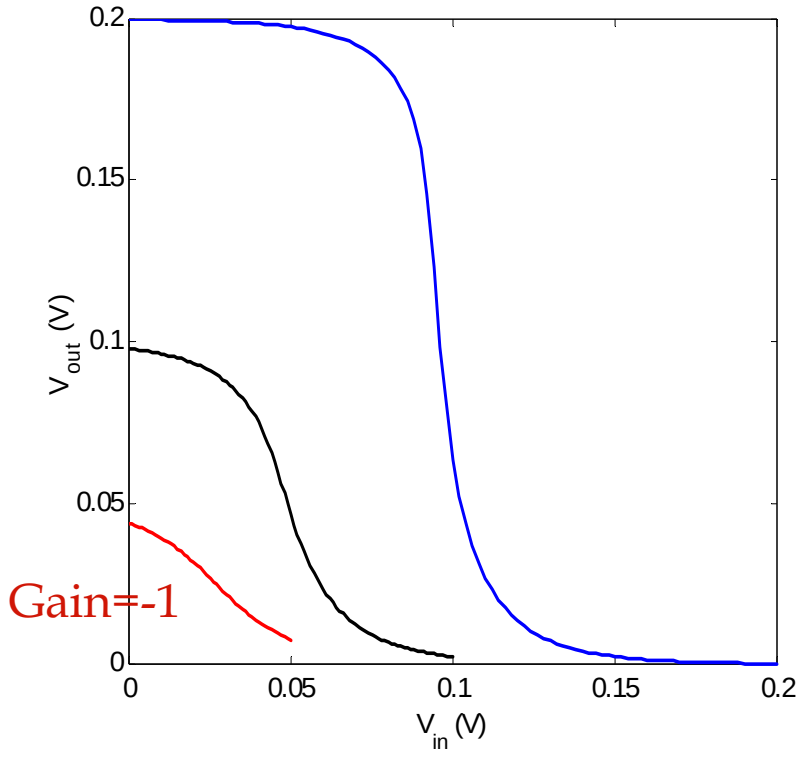


$$g = -\frac{1}{I_D(V_M)}\frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p}$$

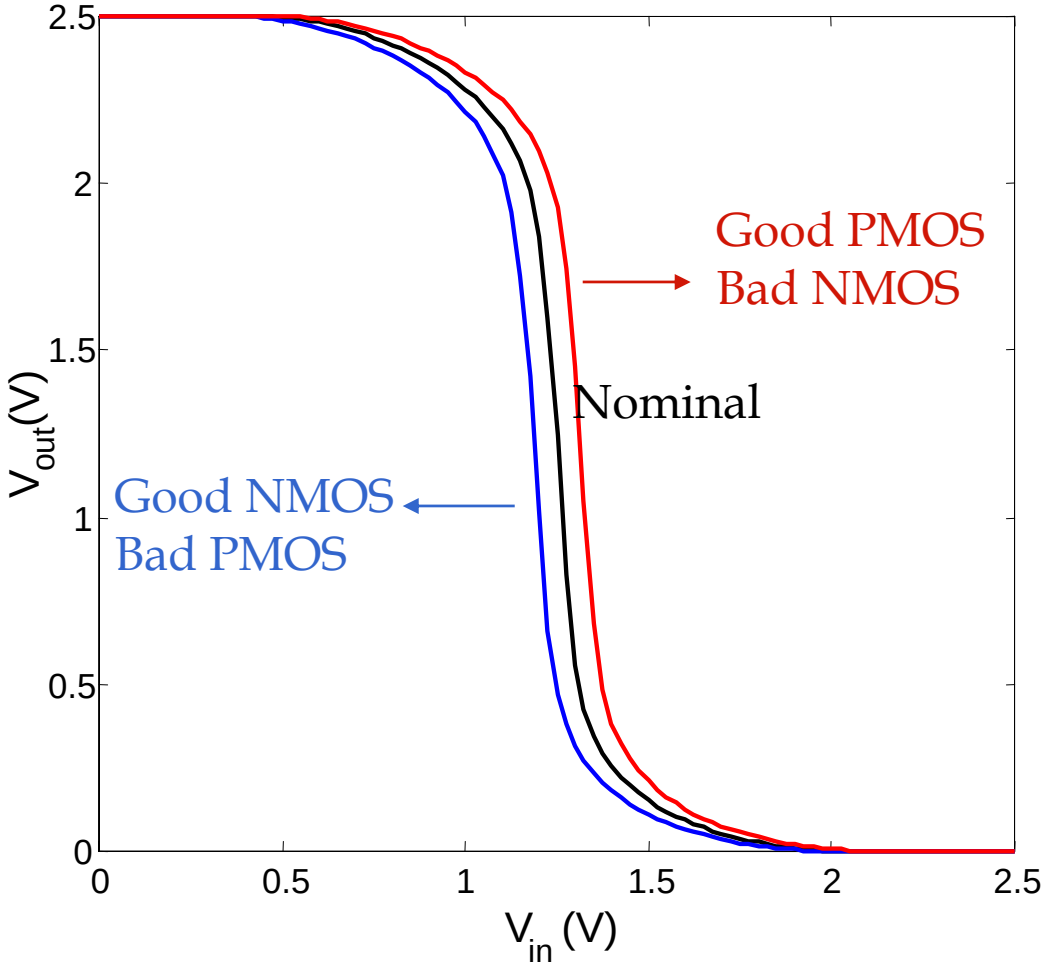
$$\approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

Gain as a function of VDD

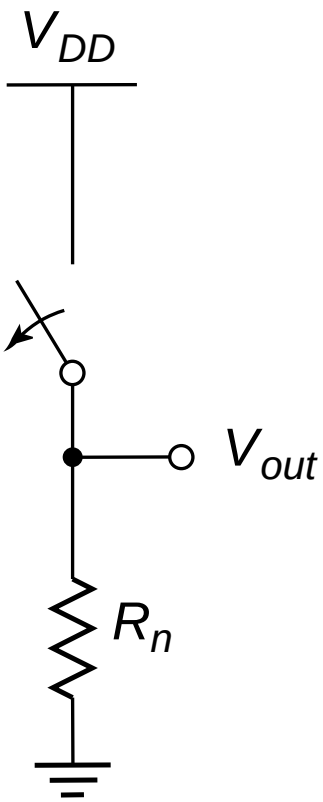




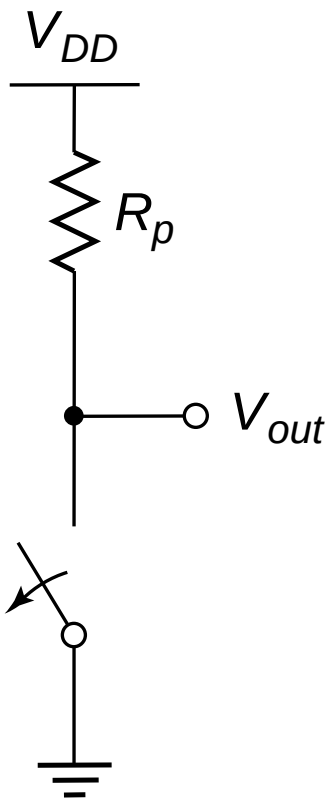
Impact of Process Variations



CMOS Inverter
First-Order DC Analysis



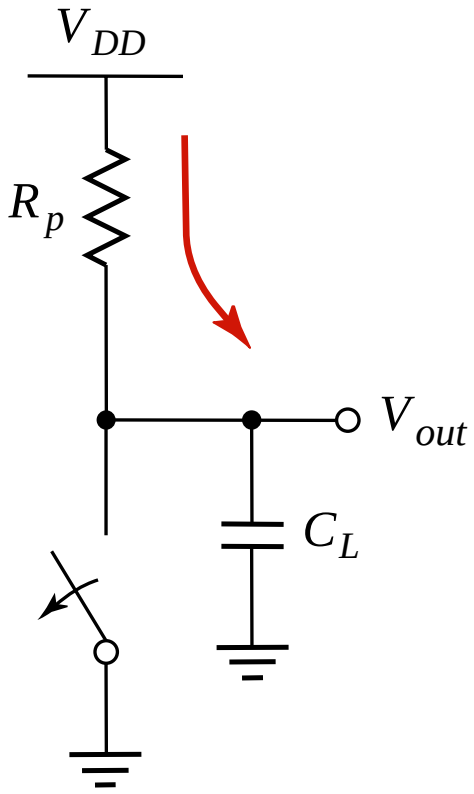
$V_{in} = V_{DD}$



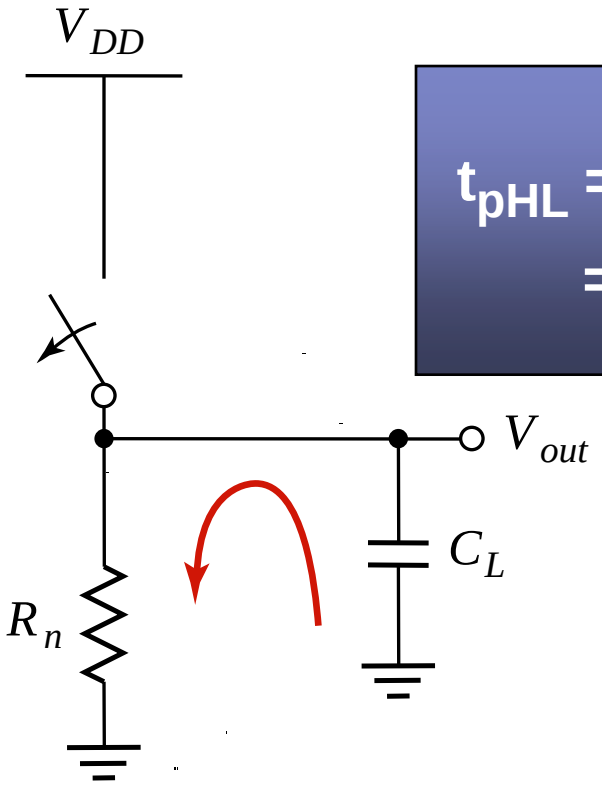
$V_{in} = 0$

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

CMOS Inverter: Transient Response



(a) Low-to-high



(b) High-to-low

$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_n\ C_L$