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Final Project: Operational Amplifier

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Introduction: An operational amplifier is designed. Several tests are conducted on it by applying analog and digital voltages to its inputs. A layout is made for the op-amp. Through the tests, much information is obtained for the op-amp. With the combination of the test information and layout, the op-amp is then ready for chip production and distribution.

Design Description/Theory: The first thing done was to design a current mirror. Using the equations I2/I1=(W2/L2)/(W1/L1), I2=2I1, and I1=(Vdd-Vgs1)/R, a current mirror with I1=10uA and I2=20uA is designed. The values obtained are W1=15um, W2=30um, L1=L2=4.95um, and R=420kohms. Using similar equations, the transistors for a diff-amp and an op-amp are determined. With the transistor widths and lengths determined, schematics of the current mirror, diff-amp, and op-amp can be created. Figure 1 contains the schematic created for the current mirror, along with its test bench on figure 2. Figure 3 contains a simulation done for testing the current mirror. The resistor value on figure 2 and the transistor on the right on figure 1 had to be adjusted to the values that they currently are so that the current mirror works the way it is suppose to. After getting the mirror to work correctly, the diff-amp schematic was prepared. Figure 4 contains this schematic, while figure 5 contains its test bench. Figure 6 contains the simulation for obtaining the diff-amp offset voltage, which upon zooming in on the figure the offset is revealed to be 13.8 mV. Figure 7 contains the op-amp schematic, while figure 8 contains its test bench. Figures 9 through 26 contain the simulations done for the op-amp. Figure 9 shows that the op-amp is a good unity-gain buffer. Figure 10 shows the input common mode range. Figure 11 shows the output voltage range. Figure 12 shows the op-amp voltage offset. Figures 11 and 12 are used to determine the open loop gain. Figure 13 shows the transfer function and phase margin of the op-amp. With this figure, the low frequency gain, the unity-gain frequency,

and the phase margin are determined. For figures 14 and 15, the op-amp had some compensation added to it by adding a capacitor. The goal was to obtain a phase margin close to 20 and 60, respectively. Figure 14 shows the margin at 20. Figure 15 shows an attempt to show the margin at 60. For figures 16 and 17, a phase value is applied to the input. Figure 18 uses a resistor for compensation in the schematic. Figure 19 contains the transient response using Rc. Figure 20 shows the total current going into vss. Figure 21 shows the common mode gain, while figure 22 shows the differential gain. They are used to determine the CMRR. Figure 23 shows the schematic for the alternate open loop method, while figure 24 has the simulation of the differential gain, starting from 1 nHz. Figure 25 shows the differential gain from 1 Hz. Figure 26 contains the graph used for determining the slew rate of the op-amp with a load attached to the output. Figure 27 contains the graph used for finding the slew rate without a load attached to the output. Figures 28 through 30 contain the layout, DRC, and LVS of the current mirror, respectively. Figures 31 through 33 contain the layout, DRC, and LVS of the diff-amp, respectively. Figures 34 through 37 contain the layout, DRC, parasitic extraction layout, and LVS of the op-amp, respectively. Figure 38 contains the transfer function simulation done after extracting the layout. Further tests are conducted on the op-amp on figures 39 and 40. These figures are used to determine the positive and negative power supply gains, respectively. With them, PSRR+ and PSRR- are determined. Figure 41 contains the layout of the op-amp in a pad frame. These figures are located on the following pages.
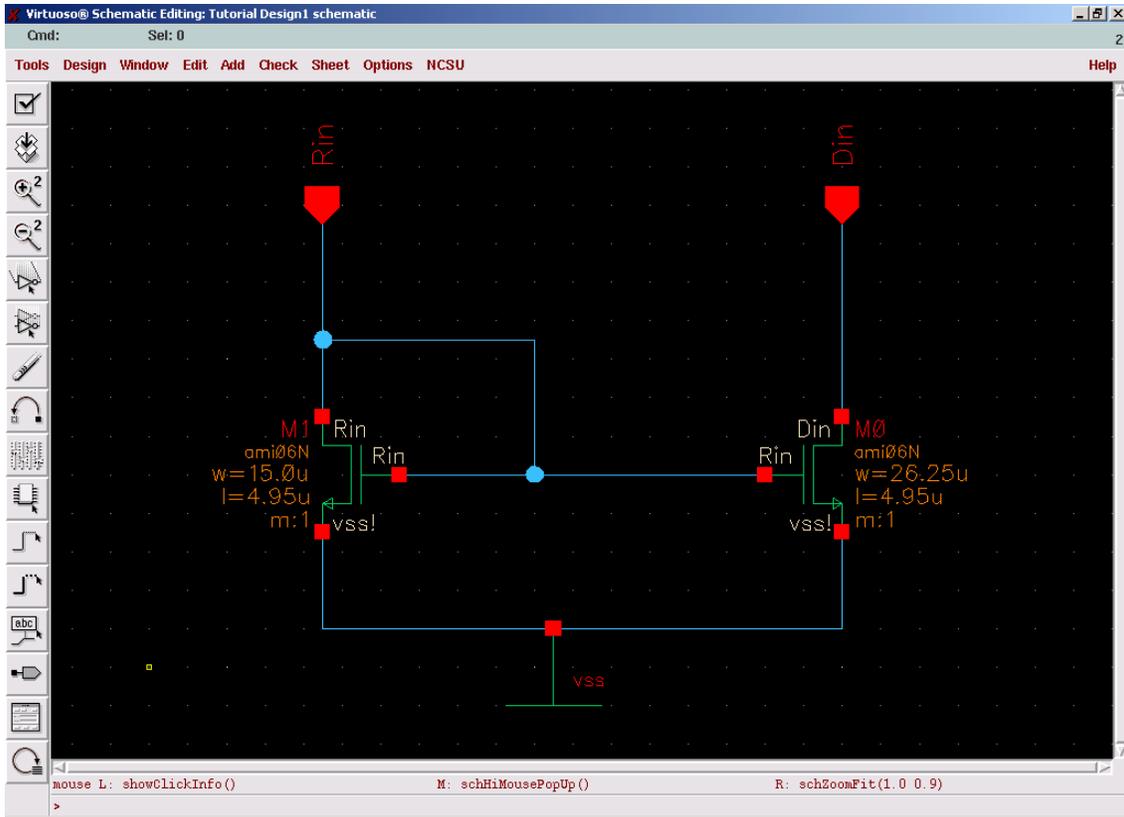
Figure 1: Current Mirror Schematic
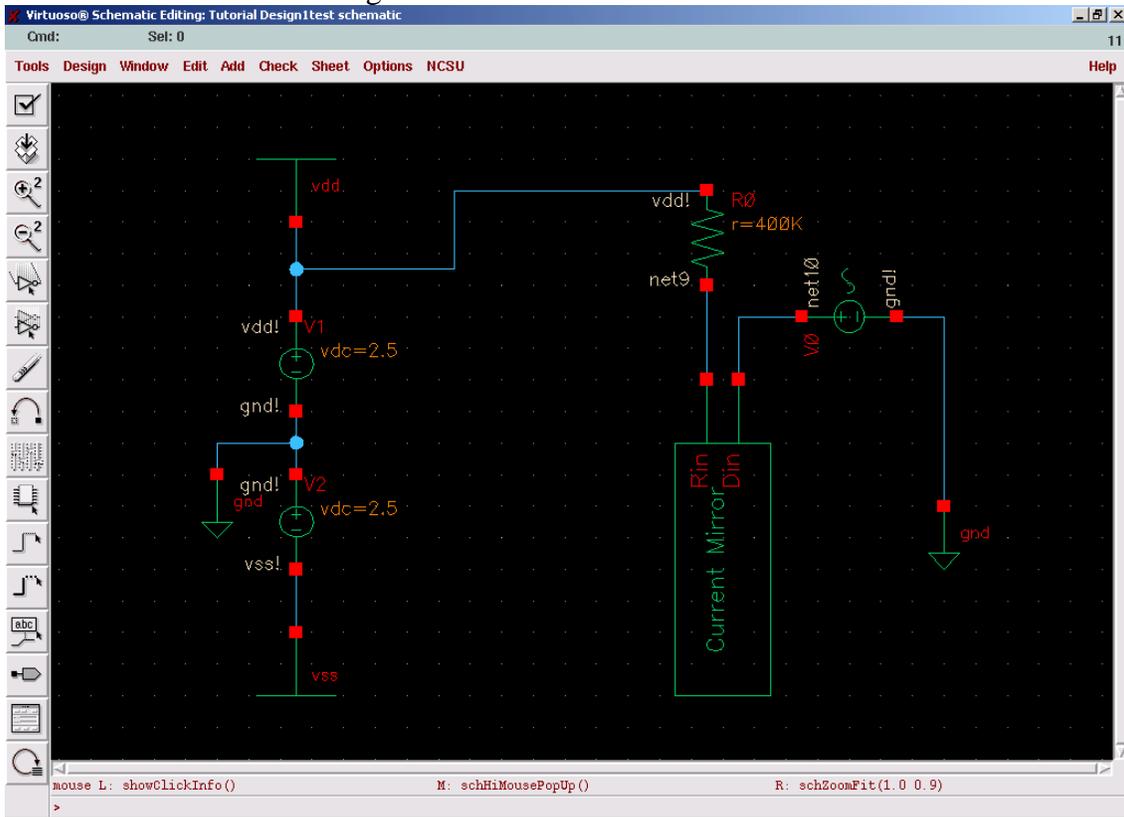
Figure 2: Current Mirror Test bench
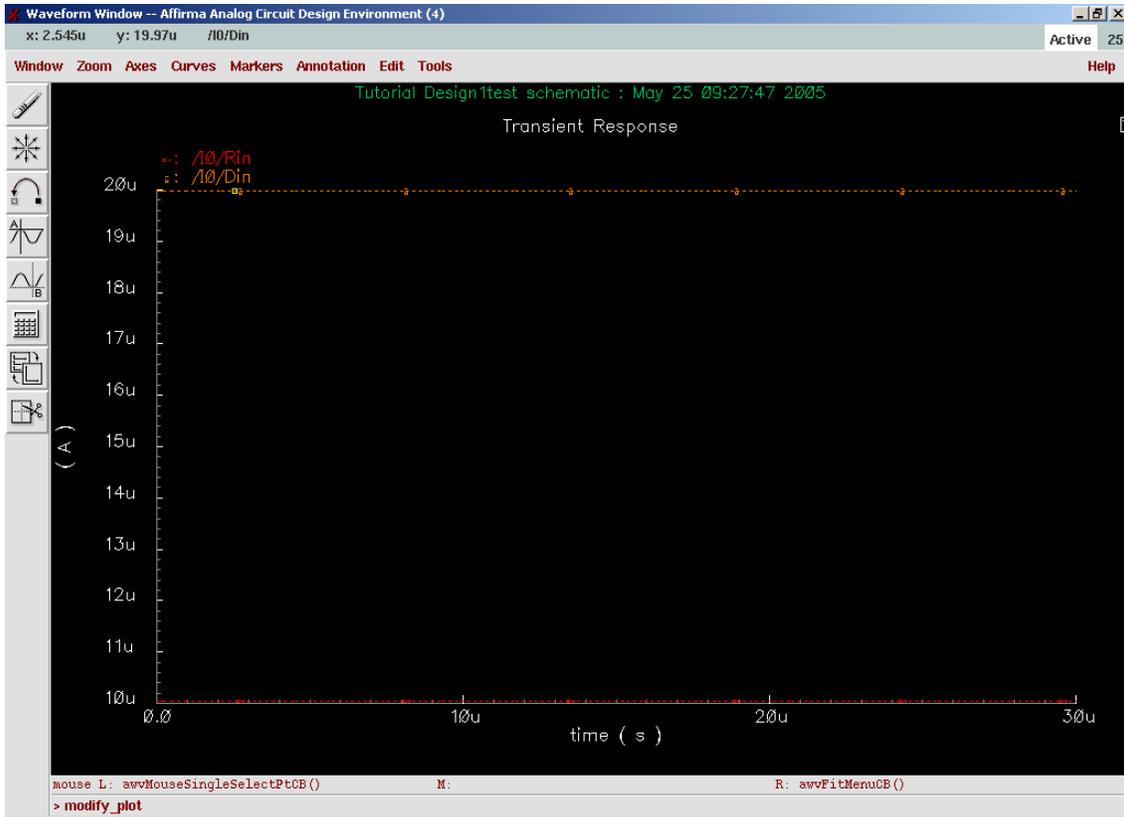
Figure 3: Current Mirror Simulation
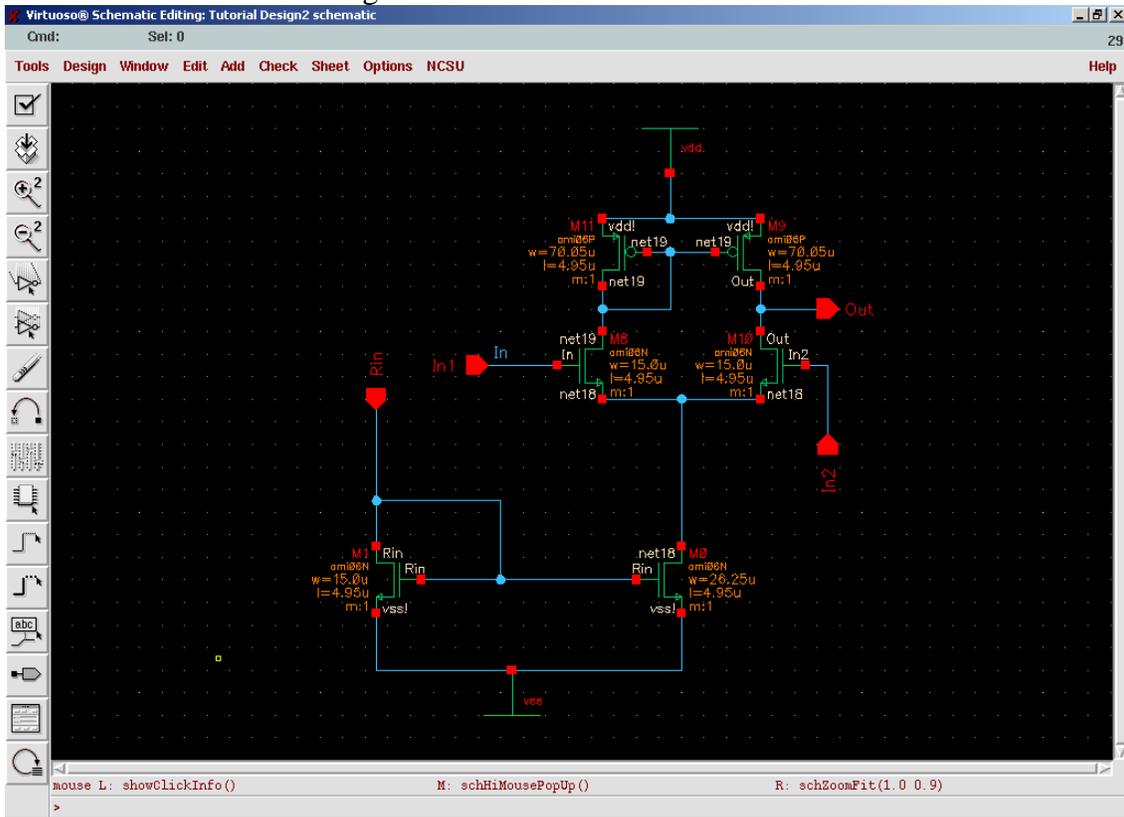
Figure 4: Diff-Amp Schematic
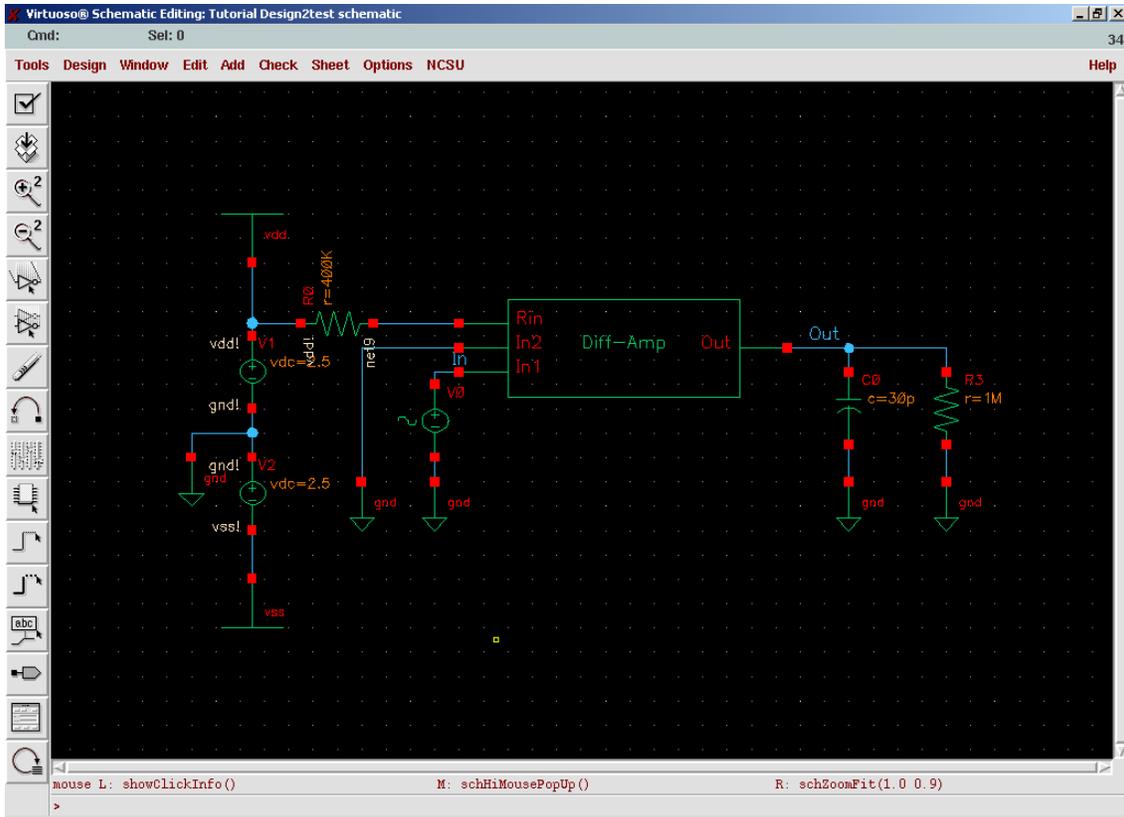
Figure 5: Diff-Amp Test bench
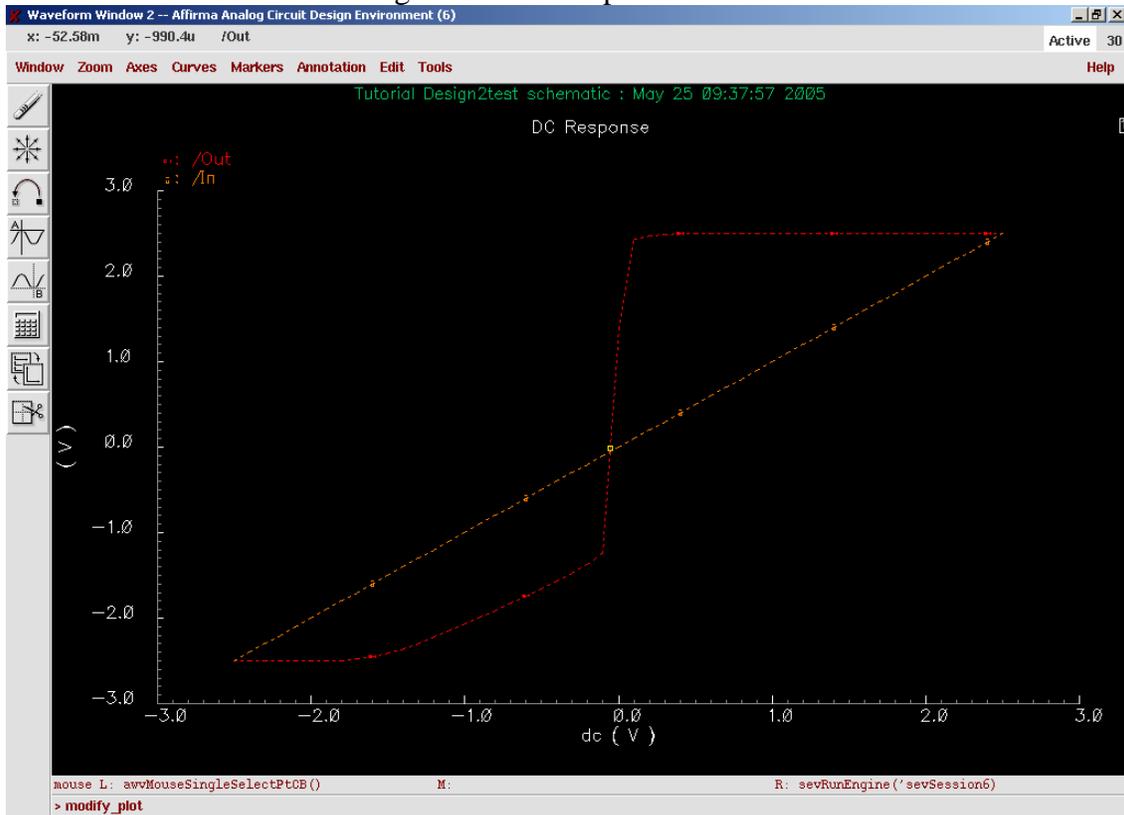
Figure 6: Diff-Amp Offset
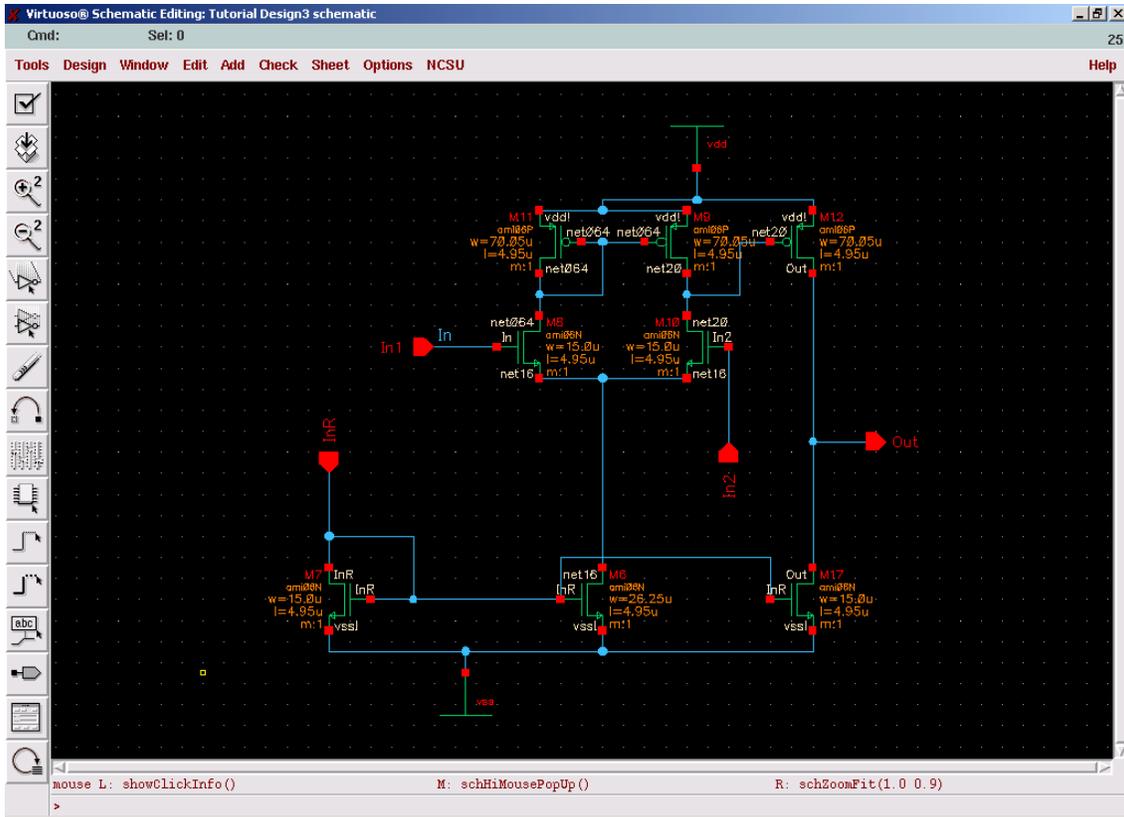
Figure 7: Op-Amp Schematic
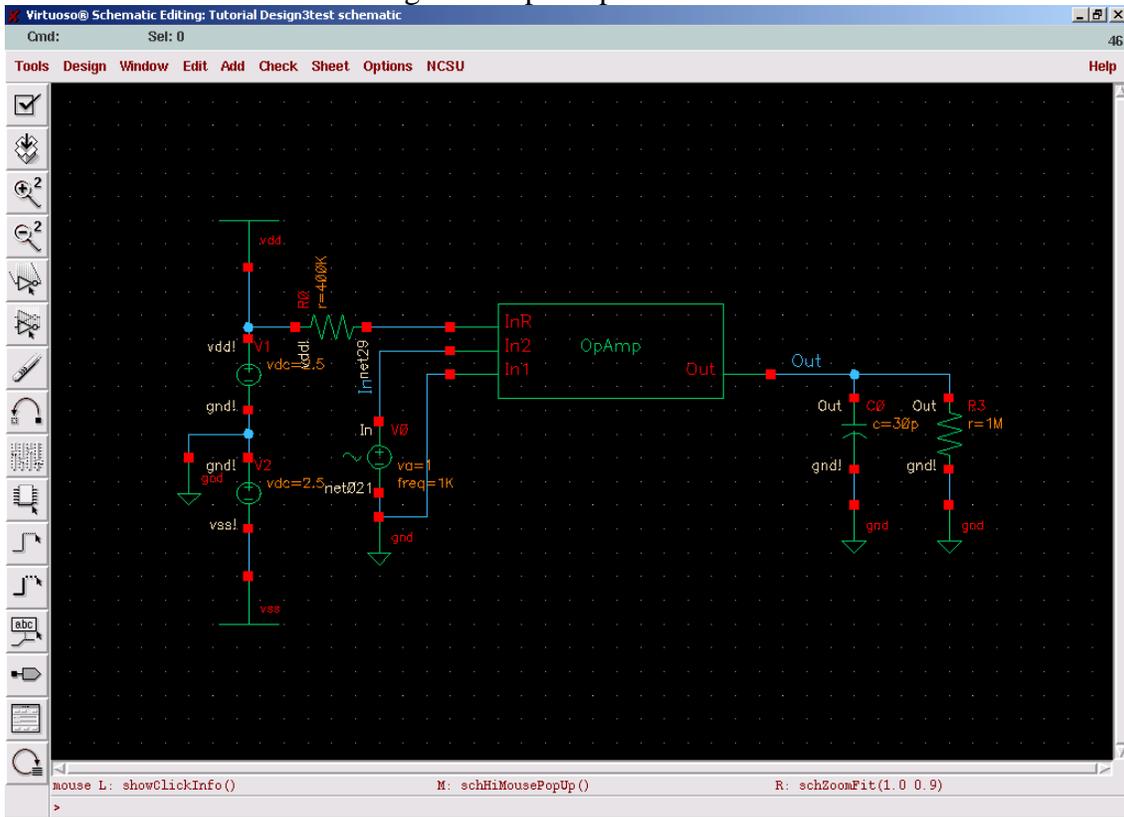
Figure 8: Op-Amp Test bench
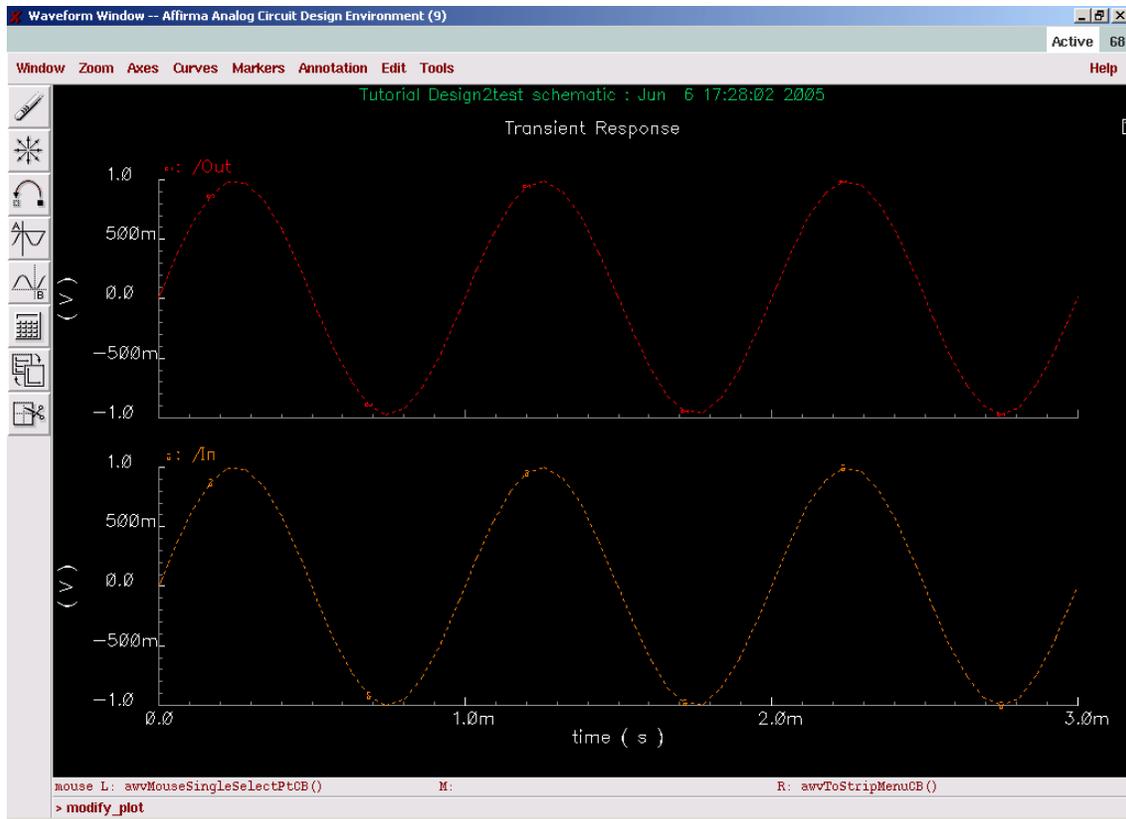
Figure 9: Plot for Showing the Unity-Gain Buffer Operation
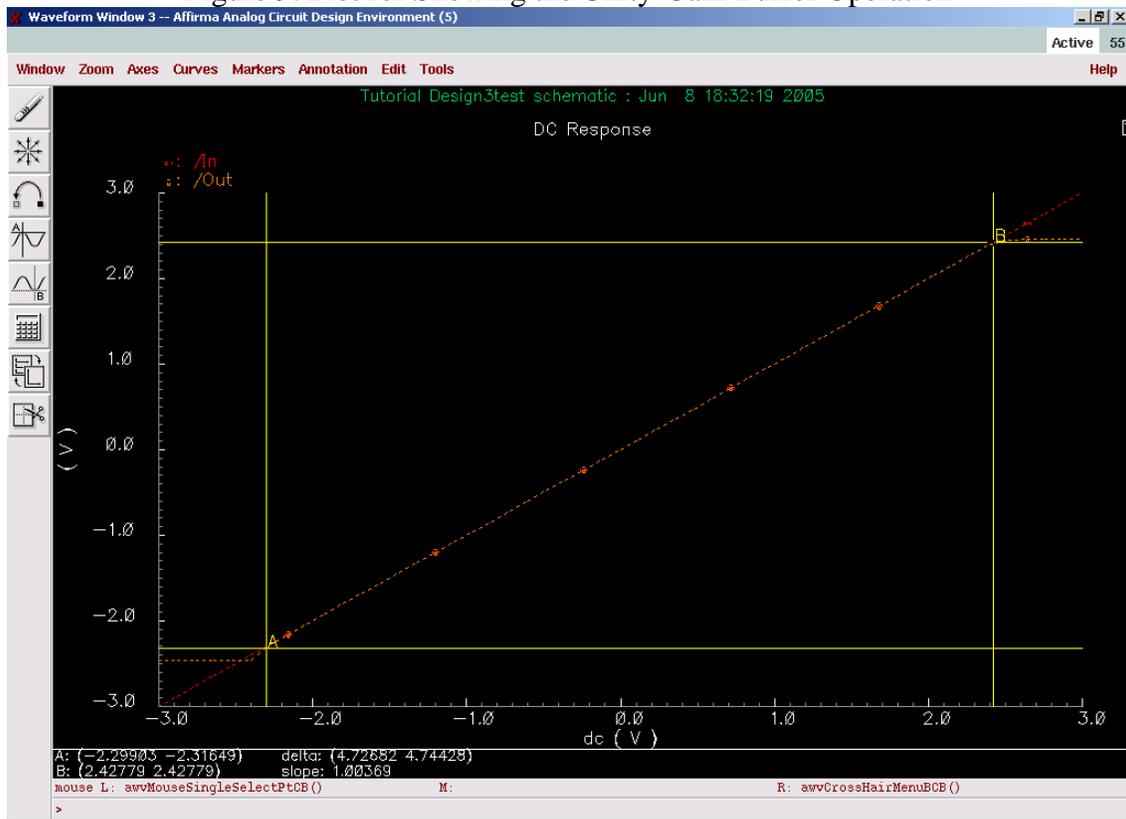
Figure 10: Simulation for Determining Input Common-Mode Range
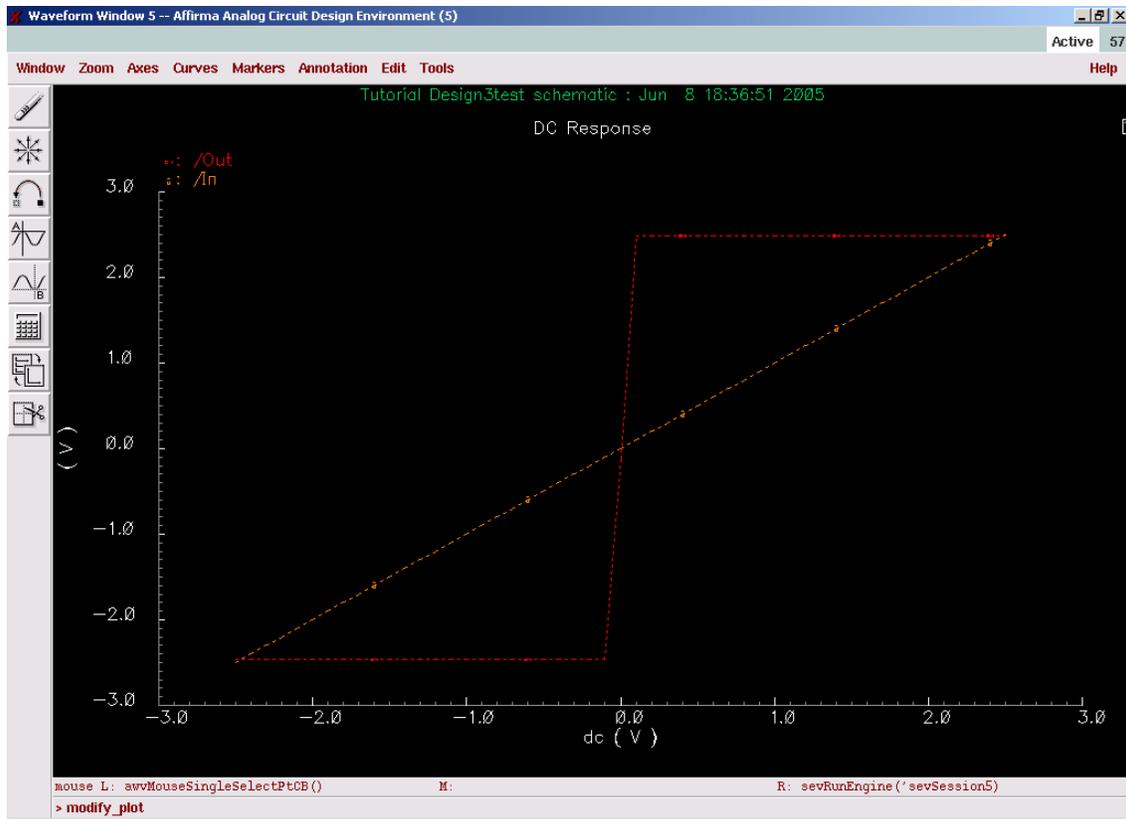
Figure 11: Simulation for Determining Output Voltage Range
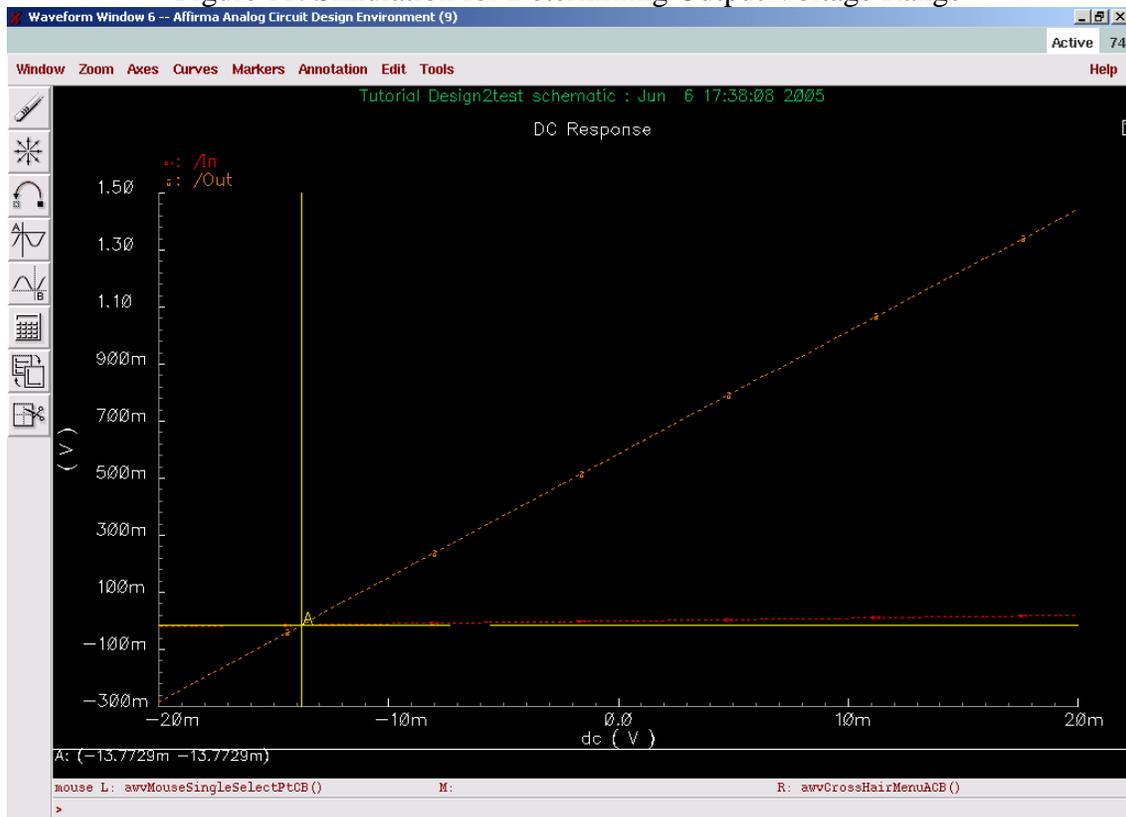
Figure 12: Simulation Showing the Op-Amp Offset: -18 uV
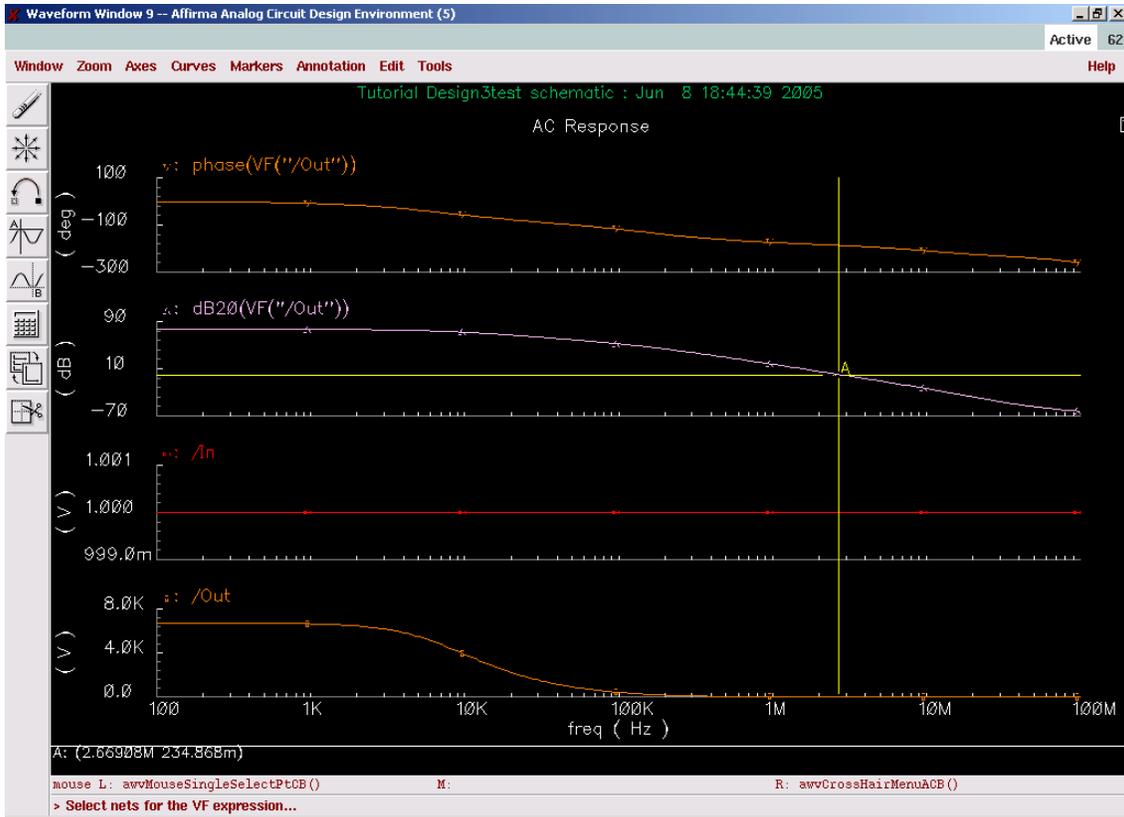
Figure 13: Simulation for Determining Transfer Function and Phase Margin
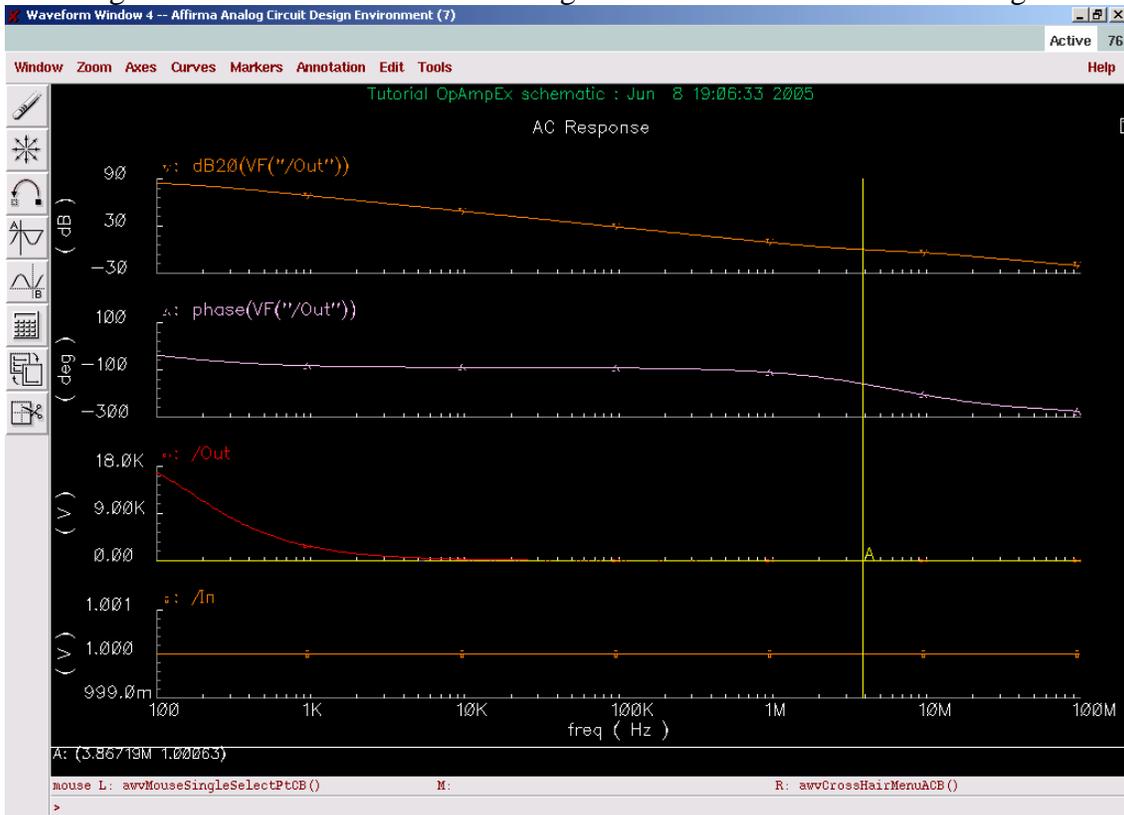
Figure 14: Simulation with Cc=4.35 pF for Getting a Phase Margin of 20
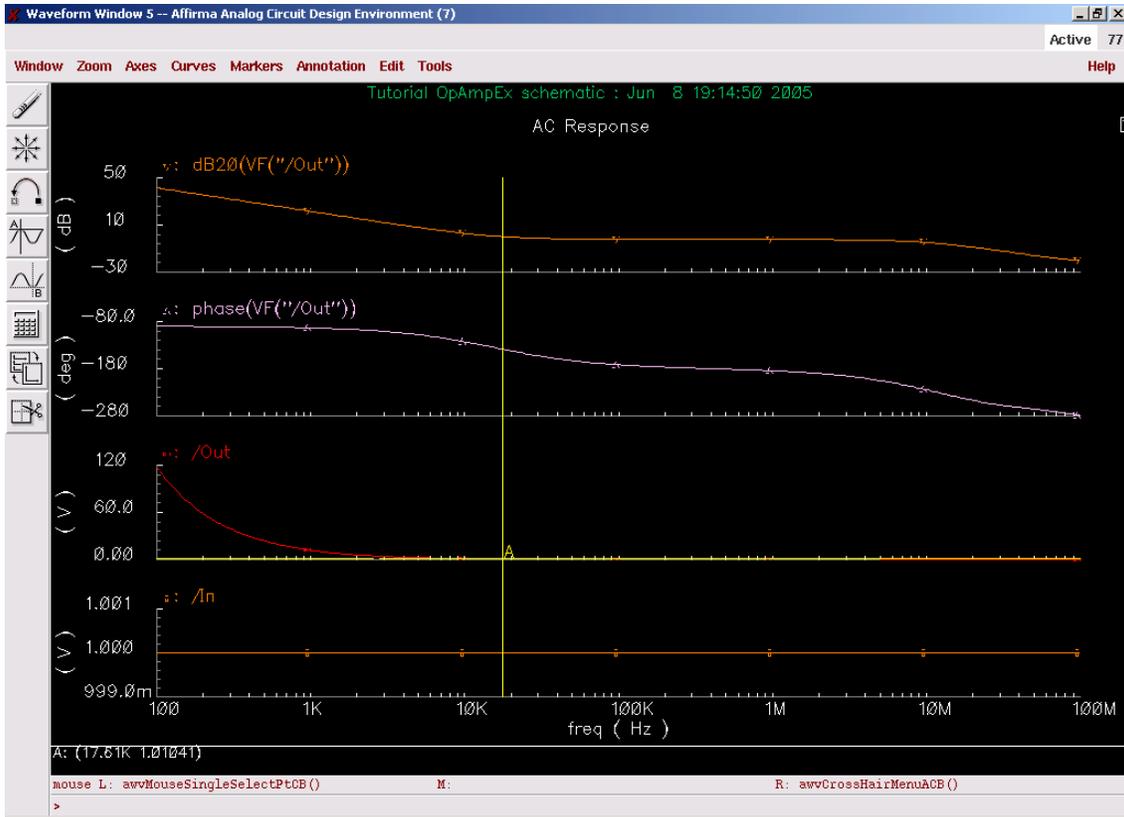
Figure 15: Simulation with Cc=1 nF for Getting a Phase Margin of 40
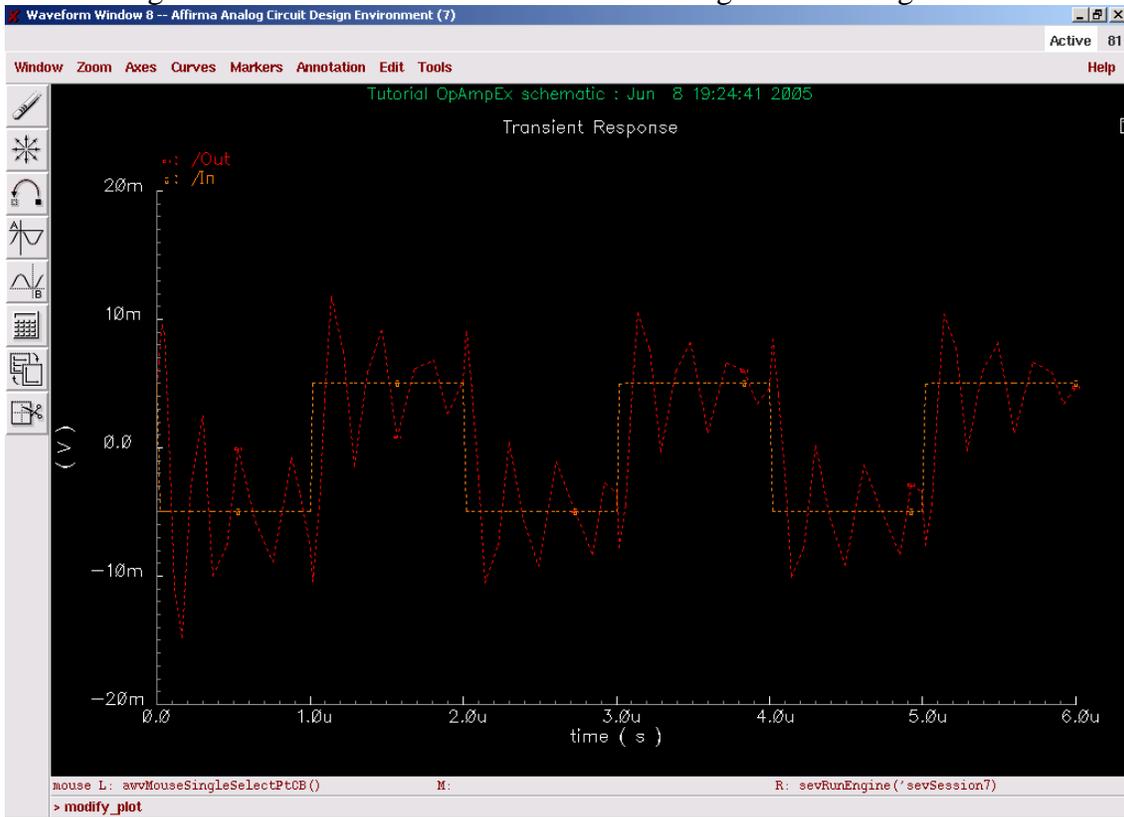
Figure 16: Transient Plot using an input with a Phase of 20 degrees
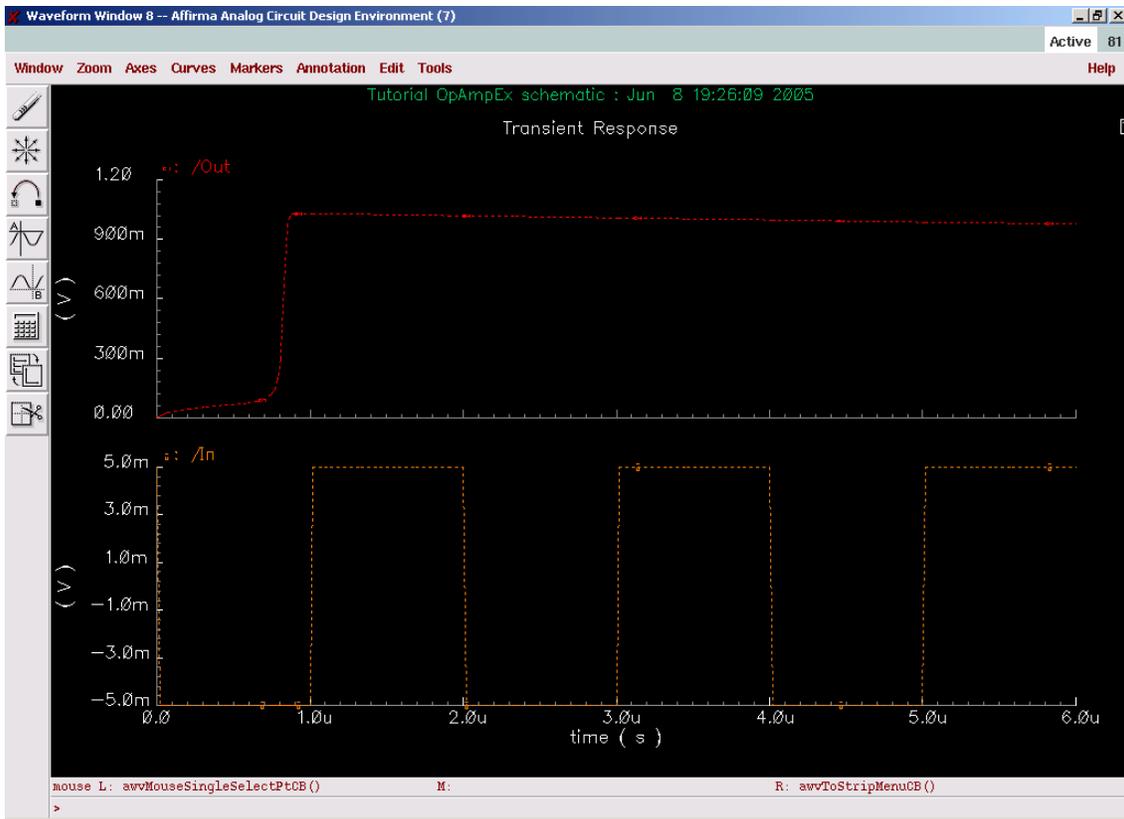
Figure 17: Transient Plot using an input with a Phase of 60 degrees
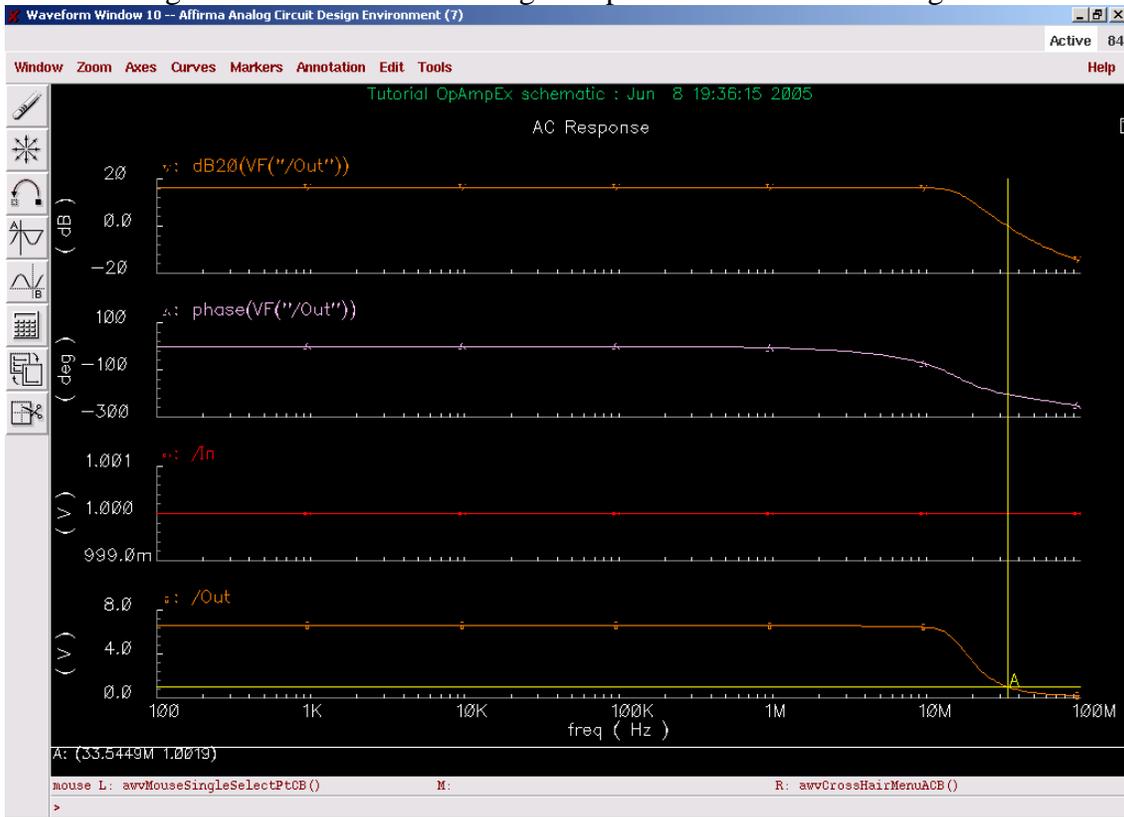
Figure 18: Amplifier Compensation Simulation using Rc=100 kohms
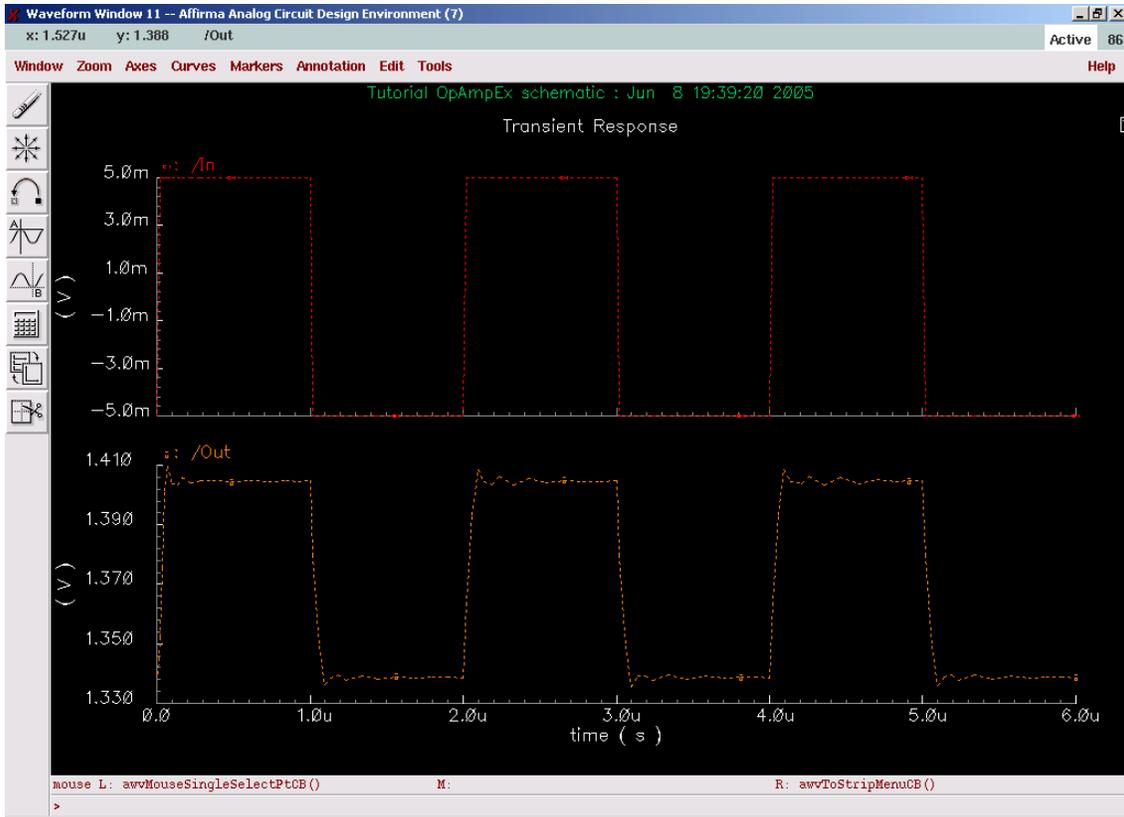
Figure 19: Transient Response of the Rc Compensated Network
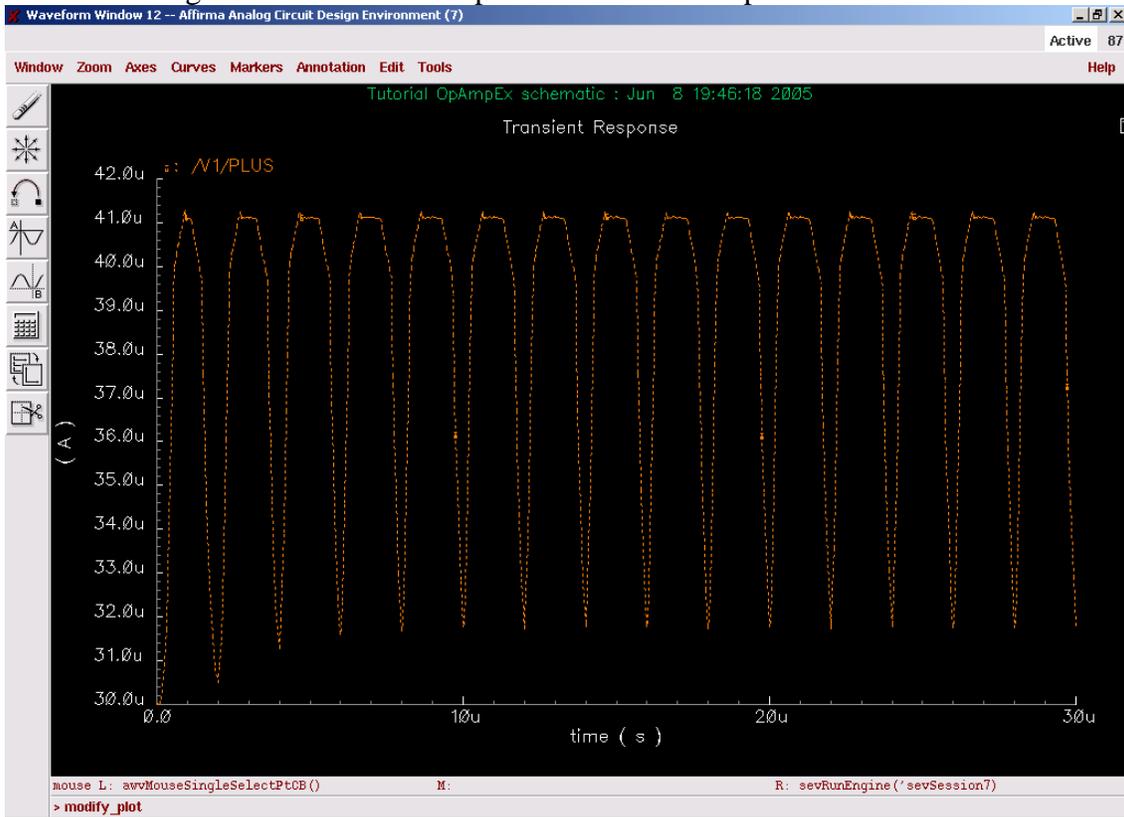
Figure 20: Plot used for Determining Total Current in the Op-Amp
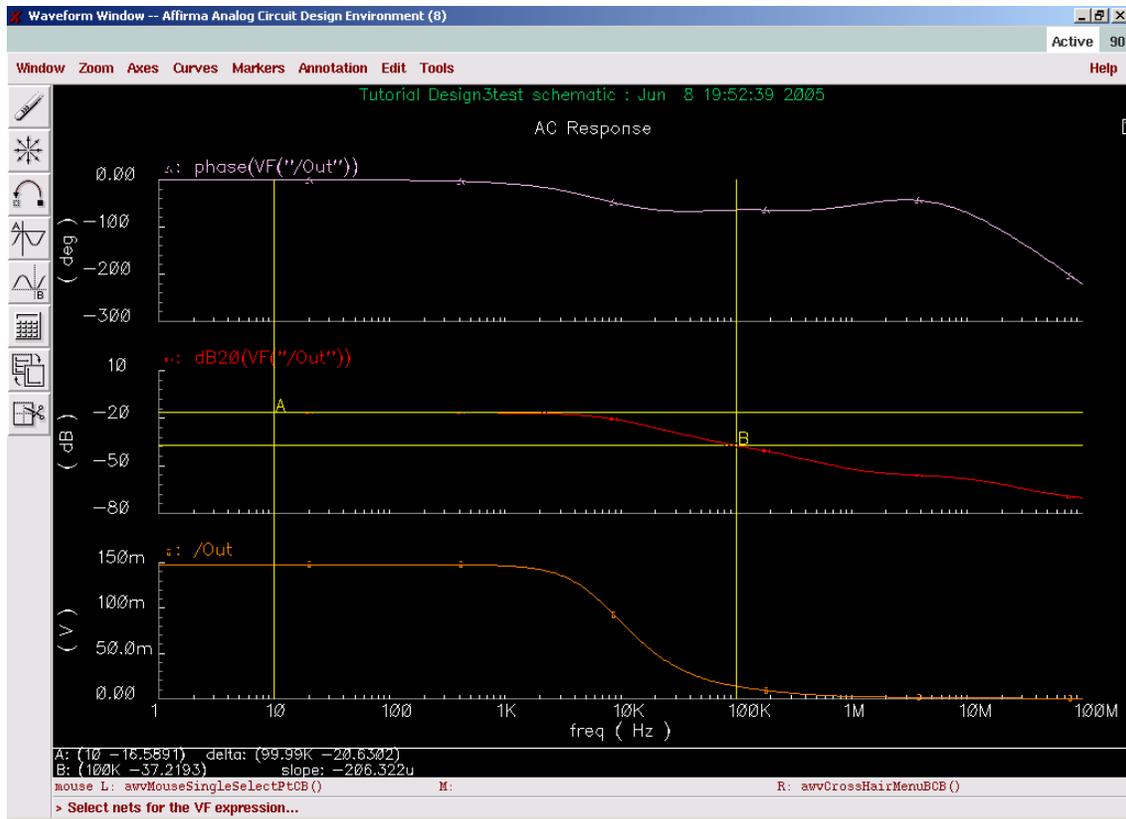
Figure 21: Plot used for Determining CM gain
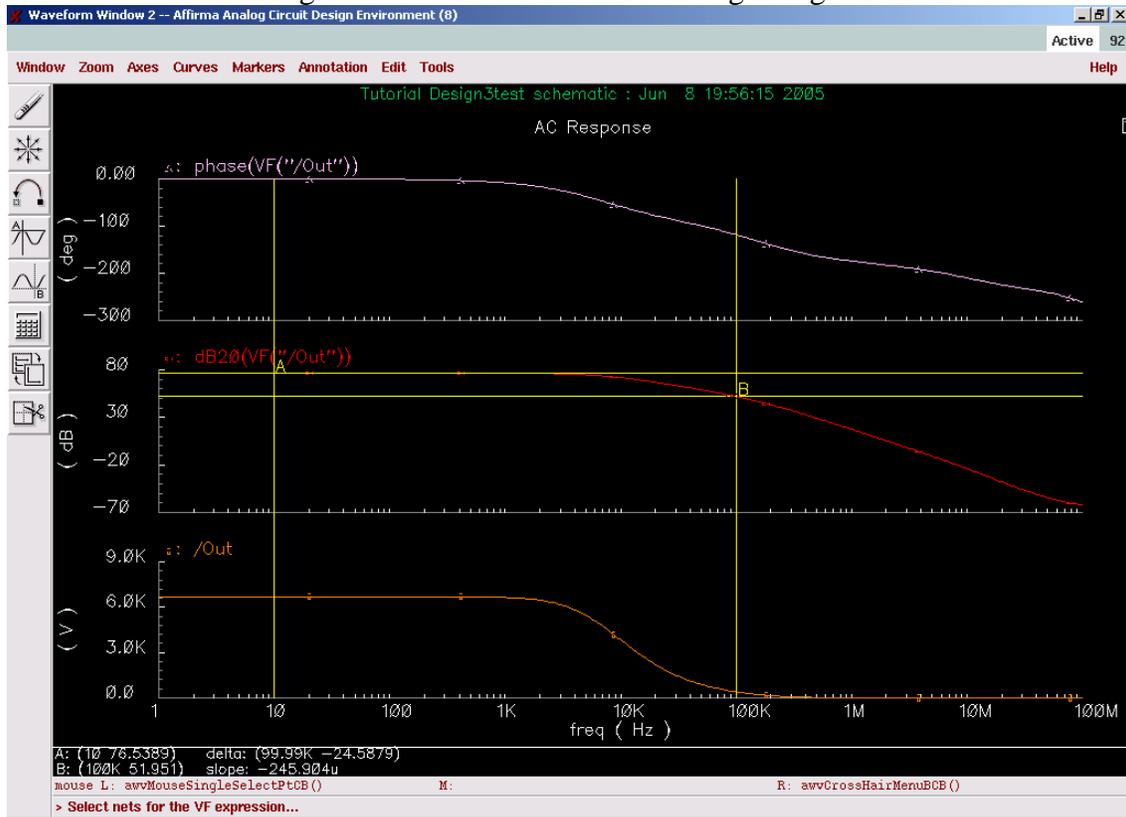
Figure 22: Plot for Finding Differential Gain
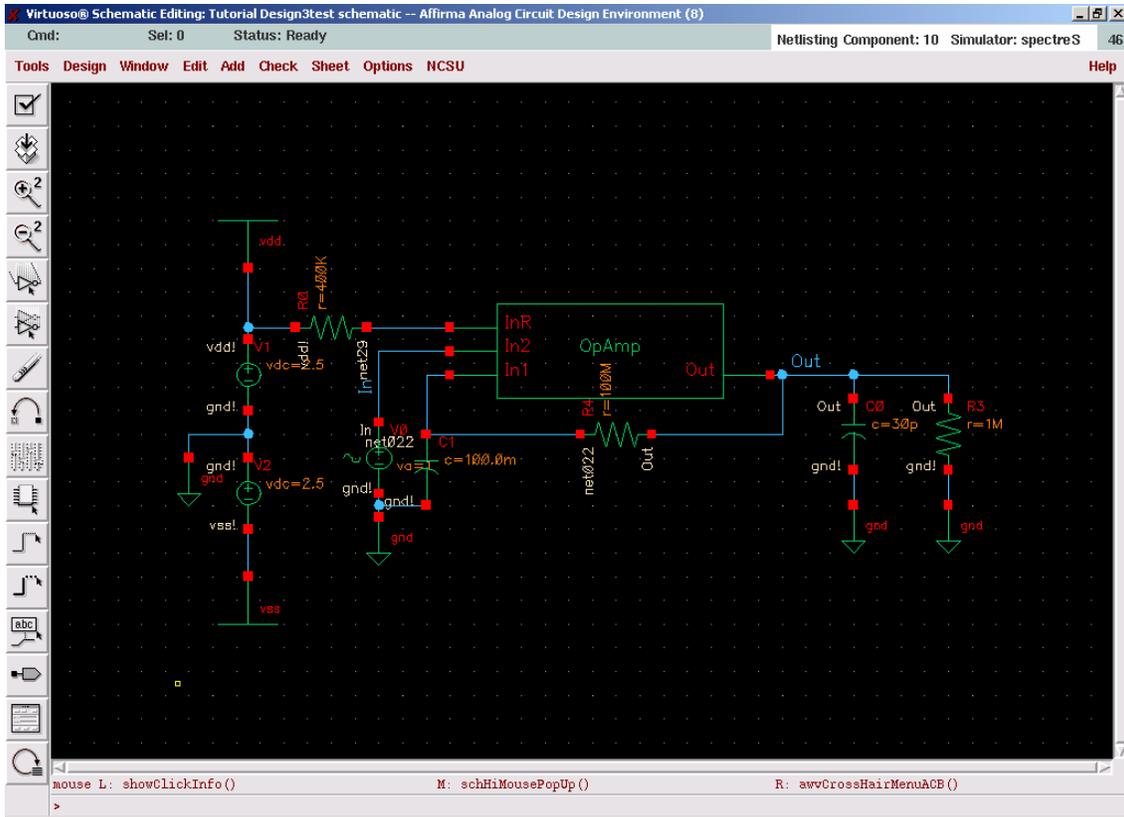
Figure 23: Alternate Open-Loop Method
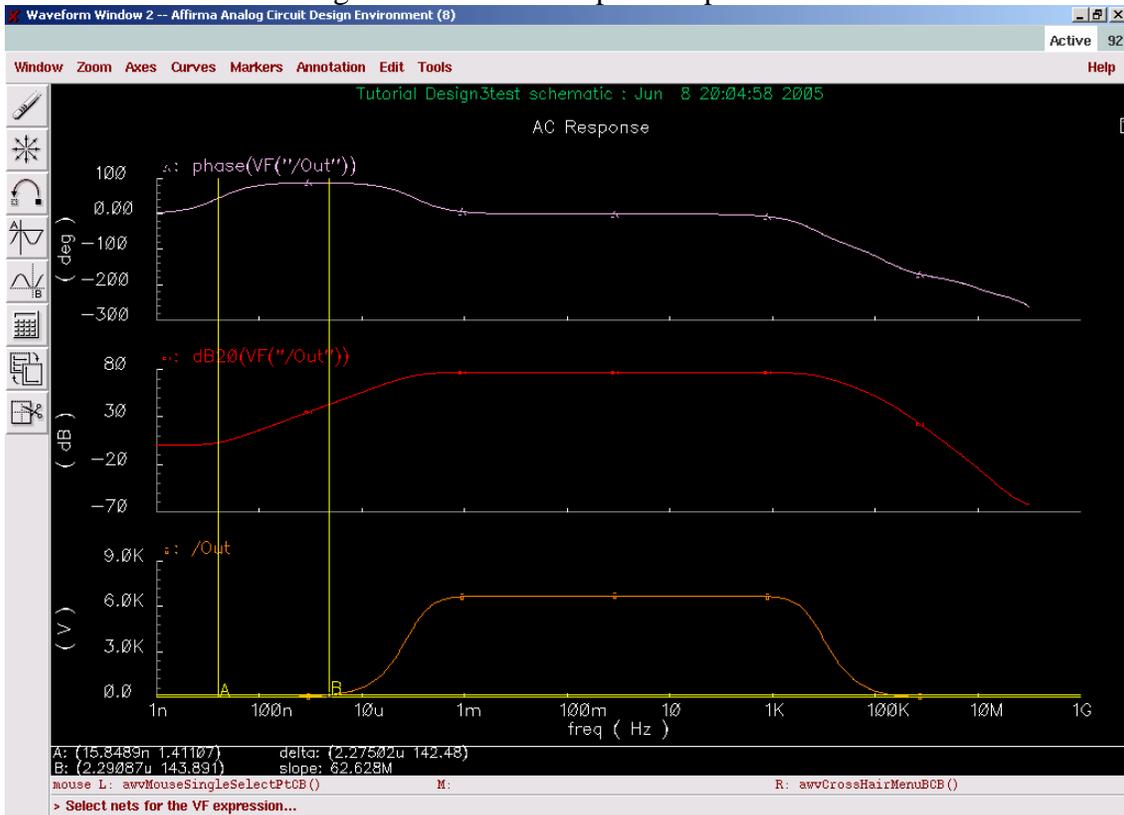
Figure 24: Alternate Method Transfer Function Simulation starting at f=1 nHz
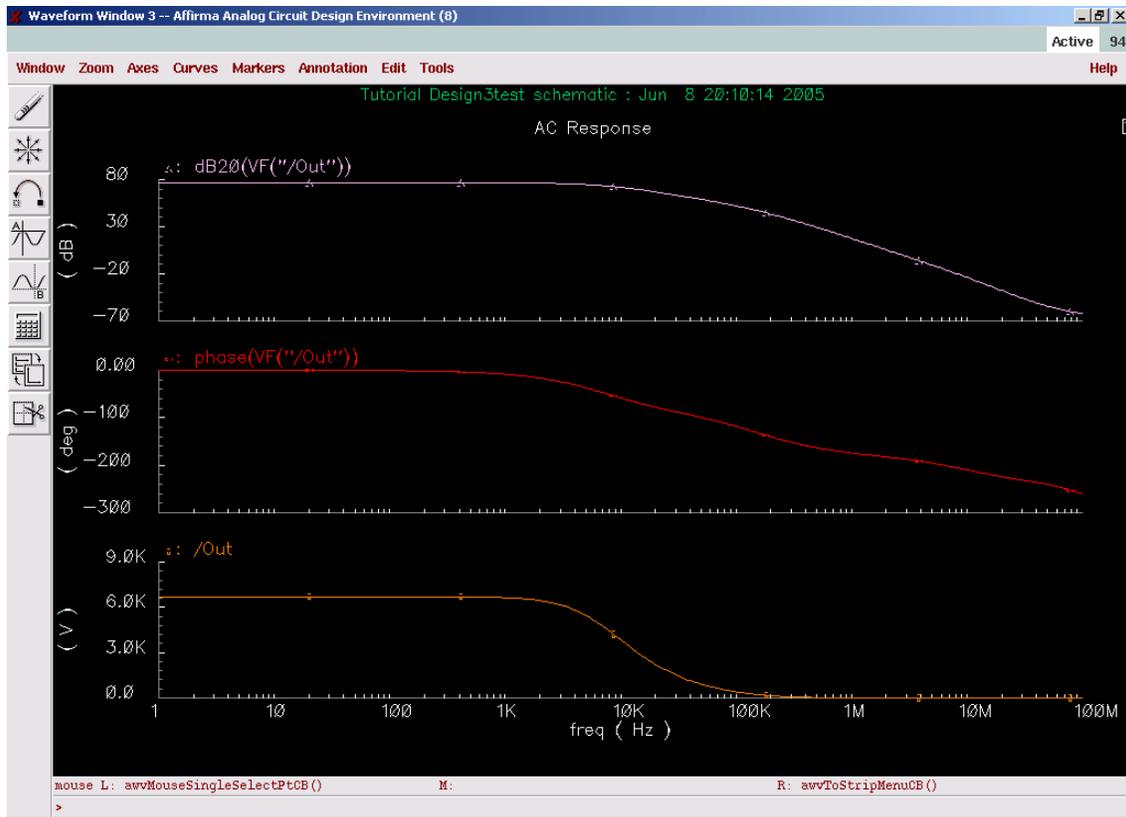
Figure 25: Alternate Method starting at f=1 Hz
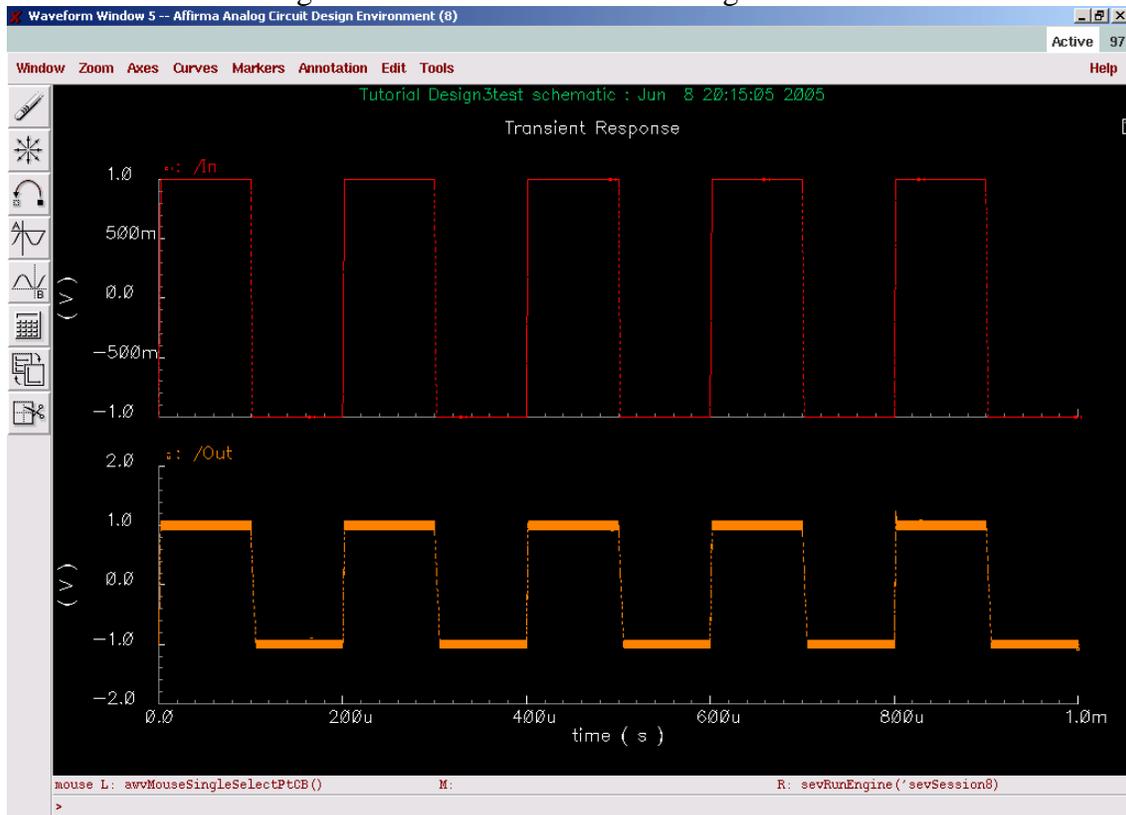
Figure 26: Plot used for Finding Slew Rate with Load
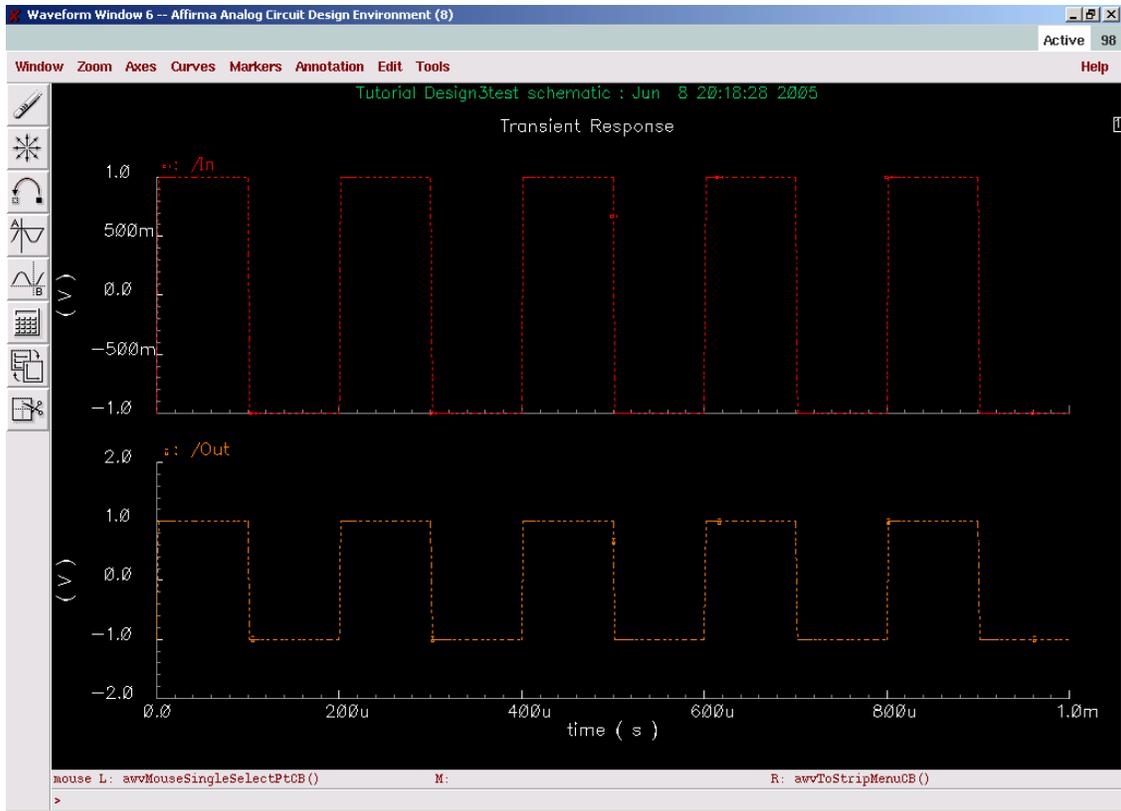
Figure 27: Plot used for Finding Slew Rate without Load

Figure 28: Current Mirror Layout

File Tools Options Technology File   Help   1

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********   Summary of rule violations for cell "CurrentMirror layout"   ********
    Total errors found: 0
*WARNING* Expected 2 items for WM_STATE, got 1
*WARNING* Expected 2 items for WM_STATE, got 1
```

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    Total errors found: 0
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mouse L: showClickInfo()   M: mousePopUp()   R: setDRCForm()

\>
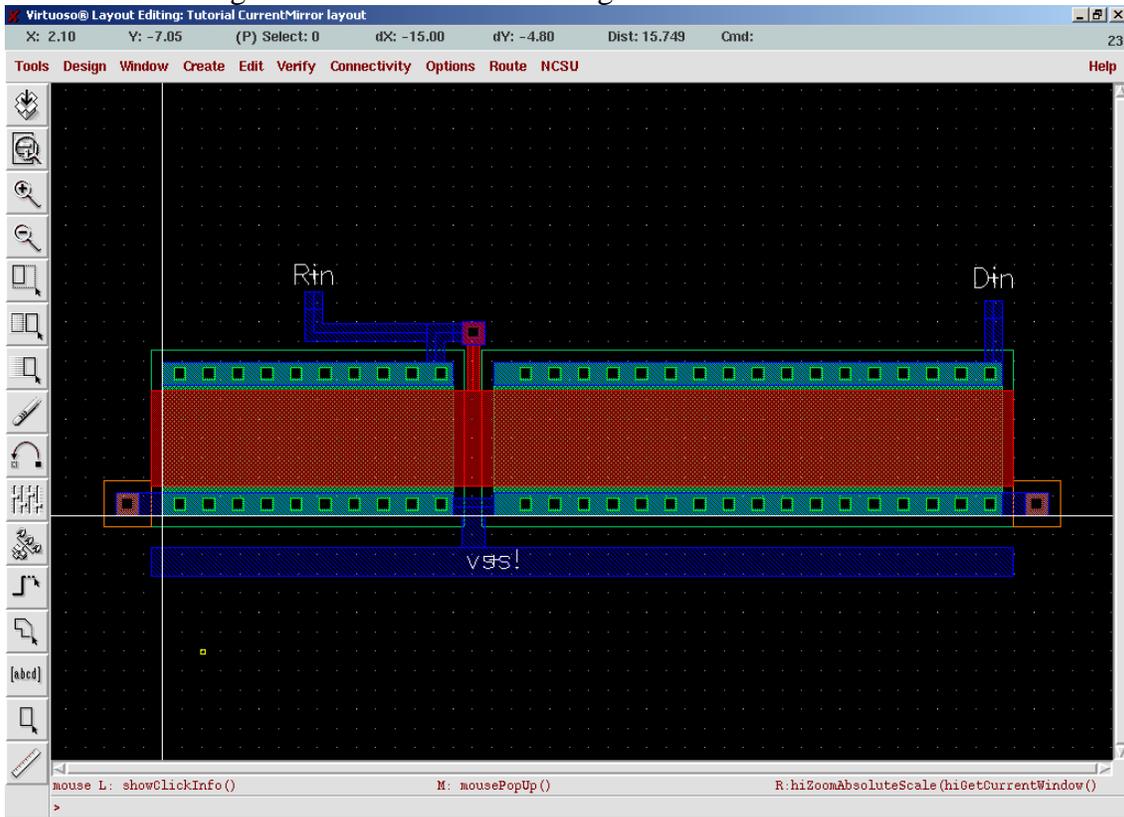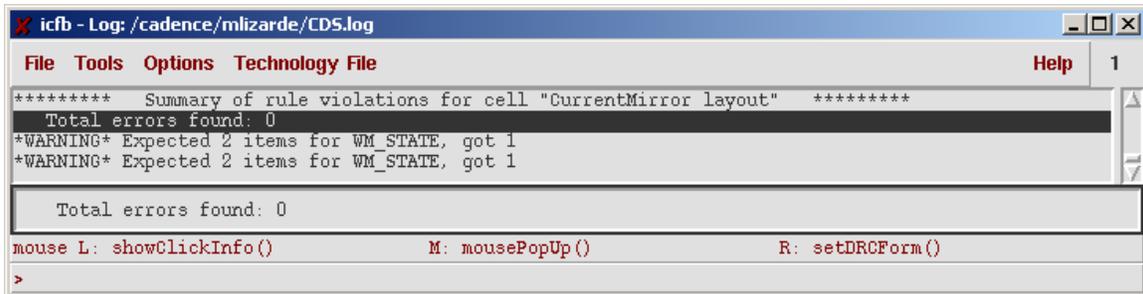
Figure 29: DRC Check of Current Mirror

File

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Compiling Diva LVS rules...

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        3           nets
        3           terminals
        2           nmos

    Net-list summary for /cadence/mlizarde/LVS/schematic/netlist
        count
        3           nets
        3           terminals
        2           nmos


    Terminal correspondence points
        1     Din
        2     Rin
        3     vss!

The net-lists match.
                        layout  schematic
                          instances
        un-matched        0        0
        rewired           0        0
        size errors       0        0
        pruned            0        0
        active            2        2
        total             2        2

                            nets
        un-matched        0        0
        merged            0        0
        pruned            0        0
        active            3        3
        total             3        3

                          terminals
        un-matched        0        0
        matched but
        different type    0        0
        total             3        3


Probe files from /cadence/mlizarde/LVS/schematic
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Figure 30: LVS Check of Current Mirror
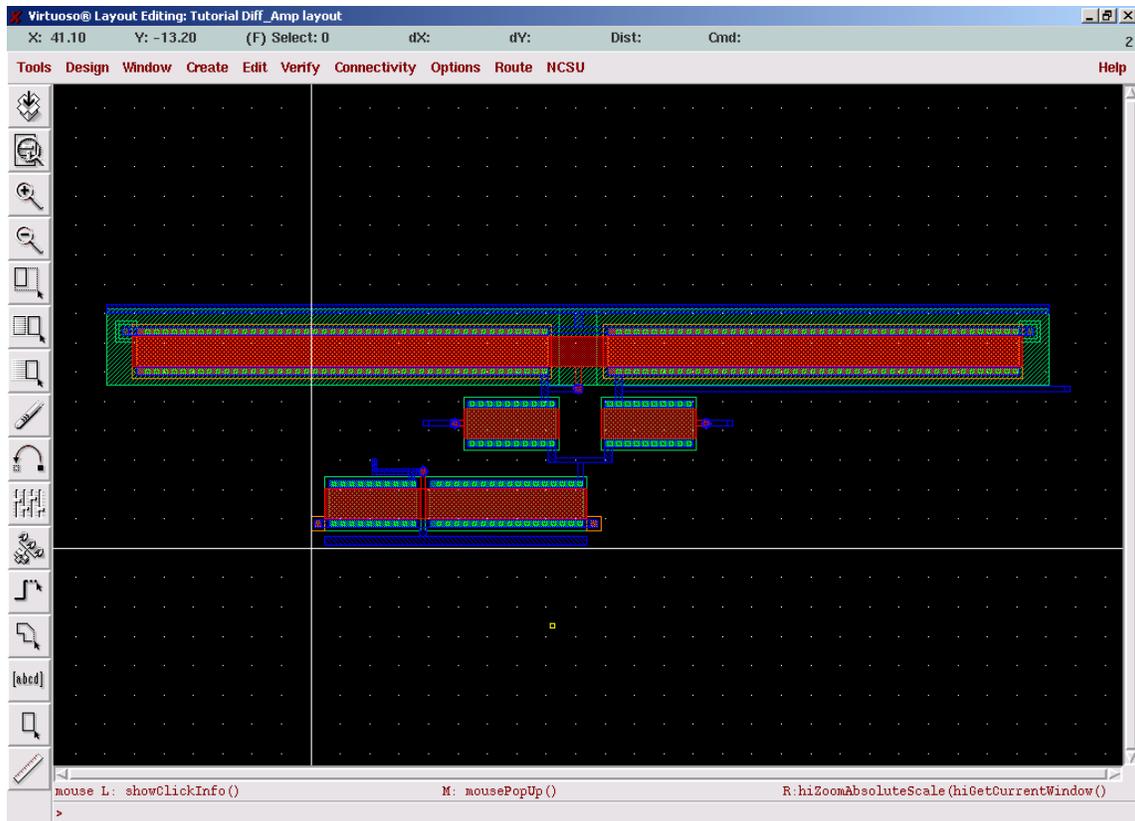
Figure 31: Diff-Amp Layout
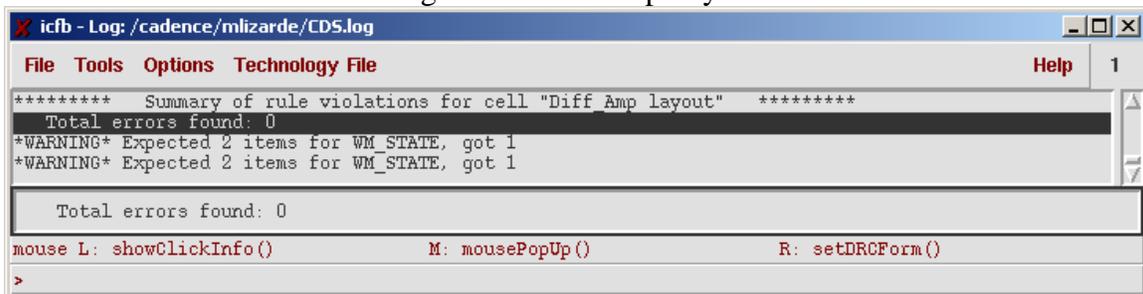
Figure 32: DRC Check of Diff-Amp

```
    Net-list summary for /cadence/mlizarde/LVS/layout/netlist
       count
       8              nets
       6              terminals
       2              pmos
       4              nmos

    Net-list summary for /cadence/mlizarde/LVS/schematic/netlist
       count
       8              nets
       6              terminals
       2              pmos
       4              nmos


    Terminal correspondence points
       1      In1
       2      In2
       3      Out
       4      Rin
       5      vdd!
       6      vss!

The net-lists match.

                        layout   schematic
                        instances
       un-matched          0        0
       rewired             0        0
       size errors         0        0
       pruned              0        0
       active              6        6
       total               6        6

                            nets
       un-matched          0        0
       merged              0        0
       pruned              0        0
       active              8        8
       total               8        8

                        terminals
       un-matched          0        0
       matched but
       different type      0        0
       total               6        6
```

Figure 33: LVS Check of Diff-Amp

Figure 34: Op-Amp Layout
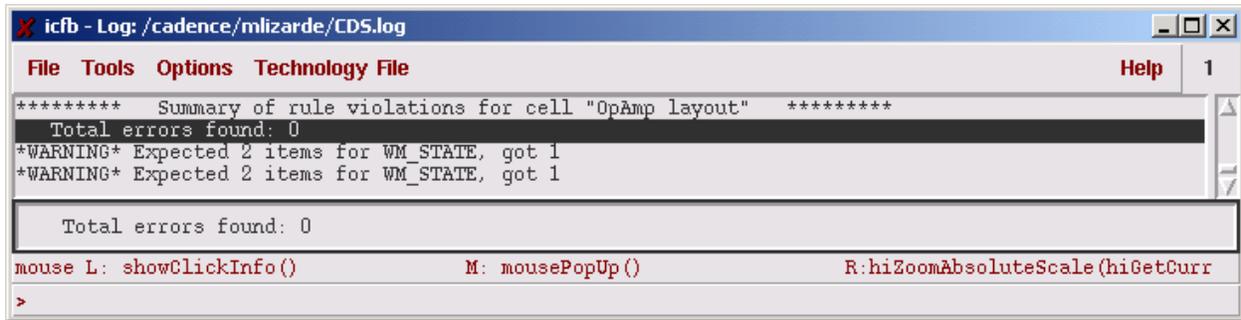
Figure 35: Op-Amp DRC Check
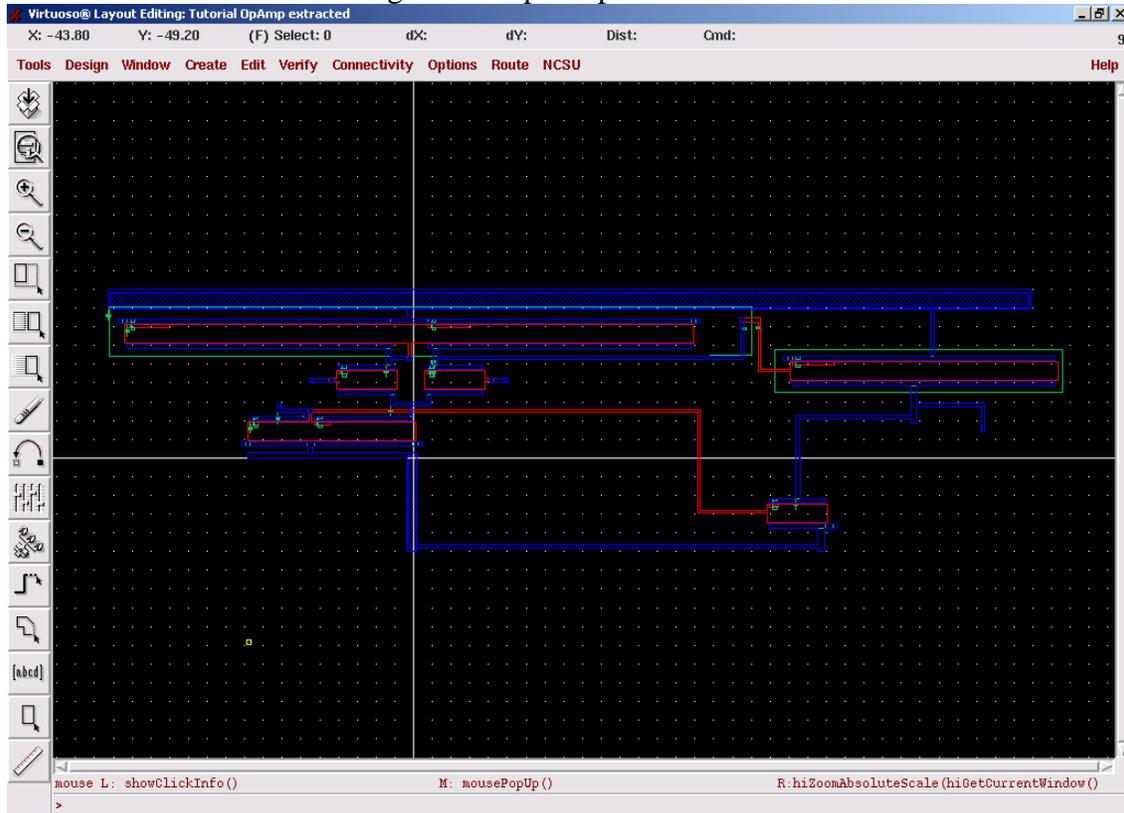
Figure 36: Op-Amp Parasitic Extraction Layout

```
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        count
          9              nets
          6              terminals
          3              pmos
          5              nmos

    Net-list summary for /cadence/mlizarde/LVS/schematic/netlist
        count
          9              nets
          6              terminals
          3              pmos
          5              nmos


    Terminal correspondence points
          1      In1
          2      In2
          3      InR
          4      Out
          5      vdd!
          6      vss!

The net-lists match.

                          layout   schematic
                            instances
        un-matched            0         0
        rewired               0         0
        size errors           0         0
        pruned                0         0
        active                8         8
        total                 8         8

                              nets
        un-matched            0         0
        merged                0         0
        pruned                0         0
        active                9         9
        total                 9         9

                           terminals
        un-matched            0         0
        matched but
        different type        0         0
        total                 6         6
```

Figure 37: Op-Amp LVS Check

Figure 38: Post Extraction Transfer Function Simulation

Figure 39: Determining Power Supply Gain (ac attached to vdd) at 10 Hz
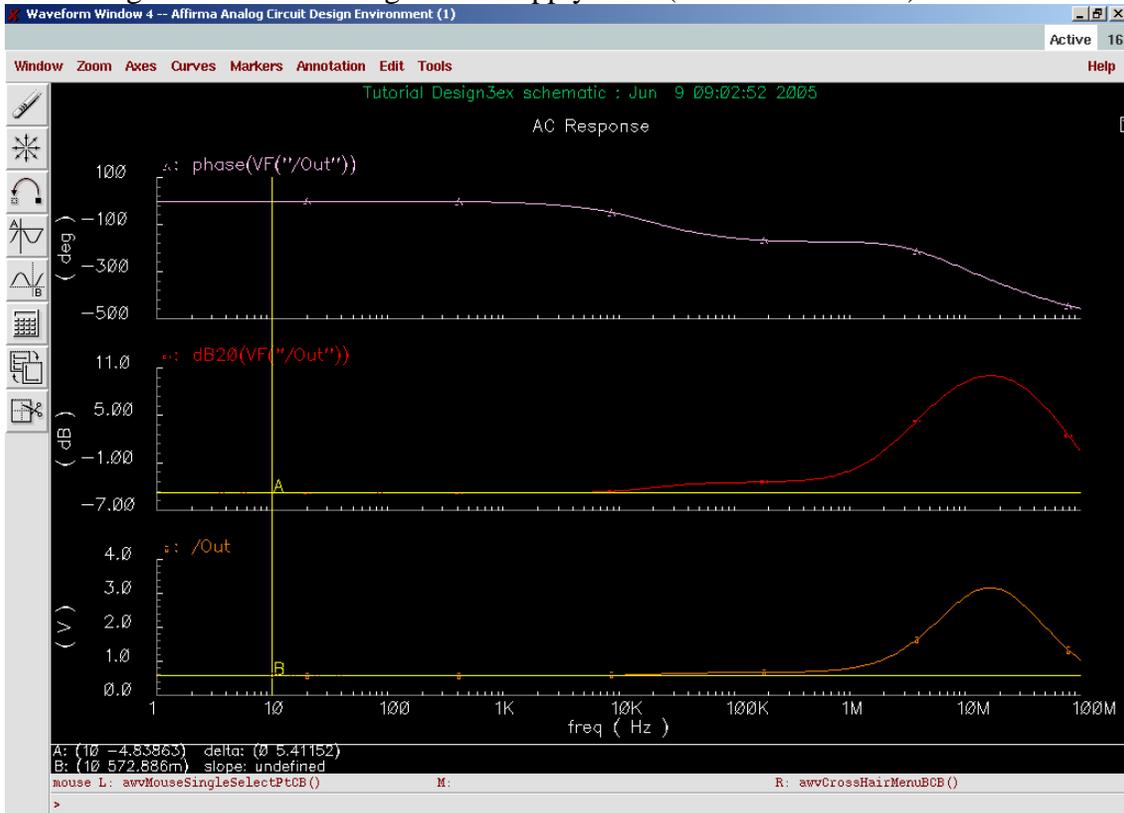
Figure 40: Determining Power Supply Gain (ac attached to vss) at 10 Hz
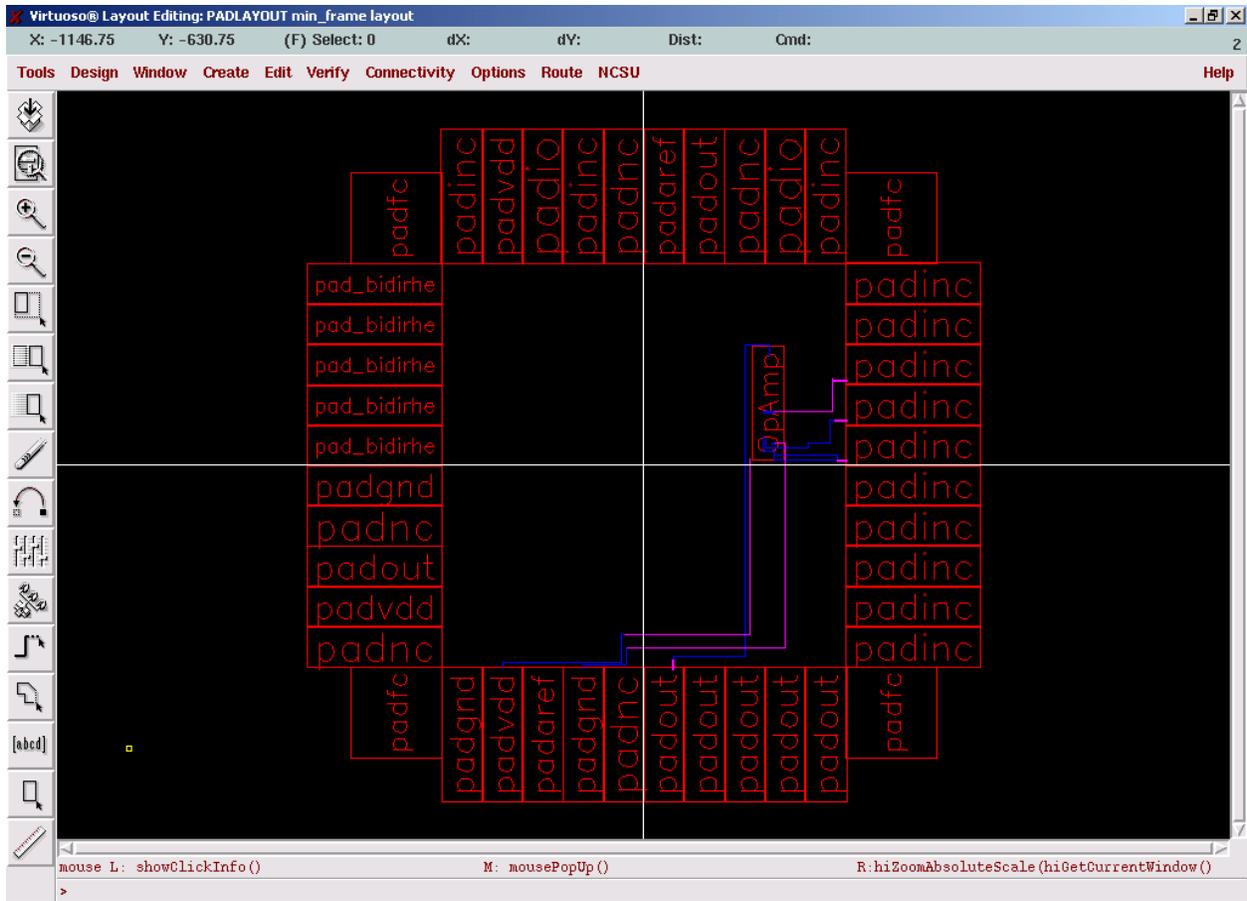
Figure 41: Pad Frame of Op-Amp

Discussion: The op-amp design at first caused many problems. It did not want to work at all. The problem was with the inputs. They were switched during the testing. After fixing this problem, everything started to work much better. The unity gain buffer worked fine. The input common-mode range of this op amp extends from the value –2.30 V to 2.43 V, as can be seen on figure 10. The output voltage range of this op amp extends from –2.47 V to 2.49 V, as can be seen on figure 11. Using figure 12, a couple of more details are acquired for the op amp. The input offset voltage for this op amp is -18 uV. The open-loop gain of this op amp is 5900 V/V. Expressing this gain in terms of dB, it is 75.4 dB. The low-frequency gain of the op amp is 76.5 dB, as can be seen on figure 13. This closely agrees with the open-loop gain measured from figure 12. It is off only by about 1 dB. Figure 13 is also used to determine a few other things. The unity-gain frequency of the op amp is 2.67 MHz, while the phase margin of the op amp is -6.2 degrees. Figure 14 shows the phase margin of 20 degrees using a compensation capacitor set at 4.35 pF. In other words, the op amp achieves a phase margin of +20 degrees with Cc=4.35 pF. Figure 15 shows a plot with a margin of 40 degrees using a compensation capacitor, Cc, set at 1nF. The attempt was to get a margin of 60, but the op-amp seems to stop at 40 degrees. As the capacitance is increased, the op-amp stays at 40 degrees. Therefore, the op amp achieves a phase margin of +60 degrees with Cc= a value that is undetermined. For the op-amp, the effect of low phase margin on the transient response is tested. Figure 16 shows a plot with the margin set at 20, in which there is a noisy output that seems to follow the input. This shows that the effect of low phase margin on the transient response is a noisy output that follows the input. Figure 17 shows a plot with the margin set at 60, where the output seems to jump to a value 1 V, and slowly go down. This shows that the effect of low phase margin on the transient response, with a phase higher then

about 40 is an output that goes and closely stays to 1 V. Phases that are too high most likely cause the op-amp to become unstable. An attempt is made for determining the resistor, Rc, for the final compensation network. It is undetermined, due to the fact that the phase margin seems to always stay negative. Therefore, the final compensation network is Rc= an undetermined value, which gives an undetermined phase margin. A transfer function simulation is shown on figure 18 with a random Rc value, 100 kohms. Since the op-amp is not responding properly to the resistor, a phase margin cannot be determined. The transient response of this compensation network shows an output that mimics the input, as figure 19 shows. It is centered at 1.37 V. It is unknown why it is centered at that point. Figure 20 shows the total current coming from the circuit and going into vss. The current seems to be centered at 36.5 uA. With this, and the total voltage of 5 V, the power dissipation of this amplifier is 180 uW. Figure 21 reveals the common mode gain of the created op-amp circuit. The common-mode gain at 10 Hz is –16.6 dB, while the common-mode gain at 100kHz is –37.2 dB. Using figure 22, the differential gain at the same frequencies is found. They are 76.5 dB and 52.0 dB, respectively. Using these values, the CMRR can be found at the two different frequencies. The CMRR at 10 Hz is 93.1 dB. The CMRR at 100 kHz is 89.2 dB. The initial and final points determined for using the alternate method of simulation, shown of figure 23, are determined to be 16 nHz and 2.323 uHz. Figure 24 shows that the first value is correct, while the second one is not. In other words, the calculated frequencies do not match the appropriate points on the curve. At 16 nHz, the dB plot begins to curve up, but at 2.323 uHz, the plot is still curving up, when it should be straightening out. Most likely, the wrong Av was used while calculating the boundary on the right. Figure 25 shows the differential-mode gain starting at 1 Hz. This gain plot compared with the differential-mode gain curve

measured in figure 22 using the traditional method is actually pretty similar. There are some slight differences, but the two are nearly the same. Figure 26 is used for calculating the positive and negative slew rates with a load attached to the output of the schematic. They are found by calculating the slope of the rise (for positive slew rate) and fall (for negative slew rate) of one pulse on the figure. The positive slew rate is 1 MV/us, and the negative slew rate is -1 MV/us. This calculation is repeated with no load attached to the schematic. Figure 27 is used. The positive slew rate with no load is 1 MV/us, and the negative slew rate with no load is -1 MV/us. The current mirror layout gave no problems. DRC and LVS checked out fine. The same goes with the diff-amp and op-amp layouts. Parasitic extraction is conducted on the op-amp, and post parasitic simulation is done. As figure 38 shows, the transfer function and gain of the simulation is very similar to the pre-extraction simulation on figure 13. This shows that the layout was correctly done. Figures 39 and 40 give a gain that lead to a large PSRR+ and PSRR-. It is uncertain whether that value is correct or not. Attaching the layout of the diff-amp to the pad frame posed only one problem, there are no vss pads on the sides. Instead, a ground pad is used. Despite these problems, the project went well.

Specs:

Input Common-Mode Range:	-2.30 V to 2.43 V
Output Voltage Range:	-2.47 V to 2.49 V
Input Offset Voltage:	-18 uV
Open-Loop Gain:	5900 V/V (75.4 dB)
Low-Frequency Gain:	76.5 dB
Unity-Gain Frequency:	2.67 MHz
Phase Margin:	-6.2 degrees
Cc for +20 degree Phase Margin:	4.35 pF
Cc for +60 degree Phase Margin:	N/A (+40 degrees is the max margin)
Rc (Compensation):	N/A (Gives negative margins)
Power Dissipation:	0.18 mW
Common-Mode Gain (10 Hz):	-16.6 dB
Common-Mode Gain (100 kHz):	-37.2 dB
CMRR (10 Hz):	93.1 dB
CMRR (100 kHz):	89.2 dB
Positive Slew Rate (with load):	1 MV/us
Negative Slew Rate (with load):	-1 MV/us
Positive Slew Rate (no load):	1 MV/us
Negative Slew Rate (no load):	-1 MV/us
PSRR+ (at 10 Hz):	14,900 V/V (83.5 dB)
PSRR- (at 10 Hz):	10,300 V/V (80.3 dB)

Pinout:

Pin 1:	400 kohm resistor (connected in series to pin 27)
Pin 2:	Positive Input
Pin 3:	Negative Input
Pin 27:	Vdd (also connected to pin 1)
Pin 29:	Vss
Pin 31:	Vout
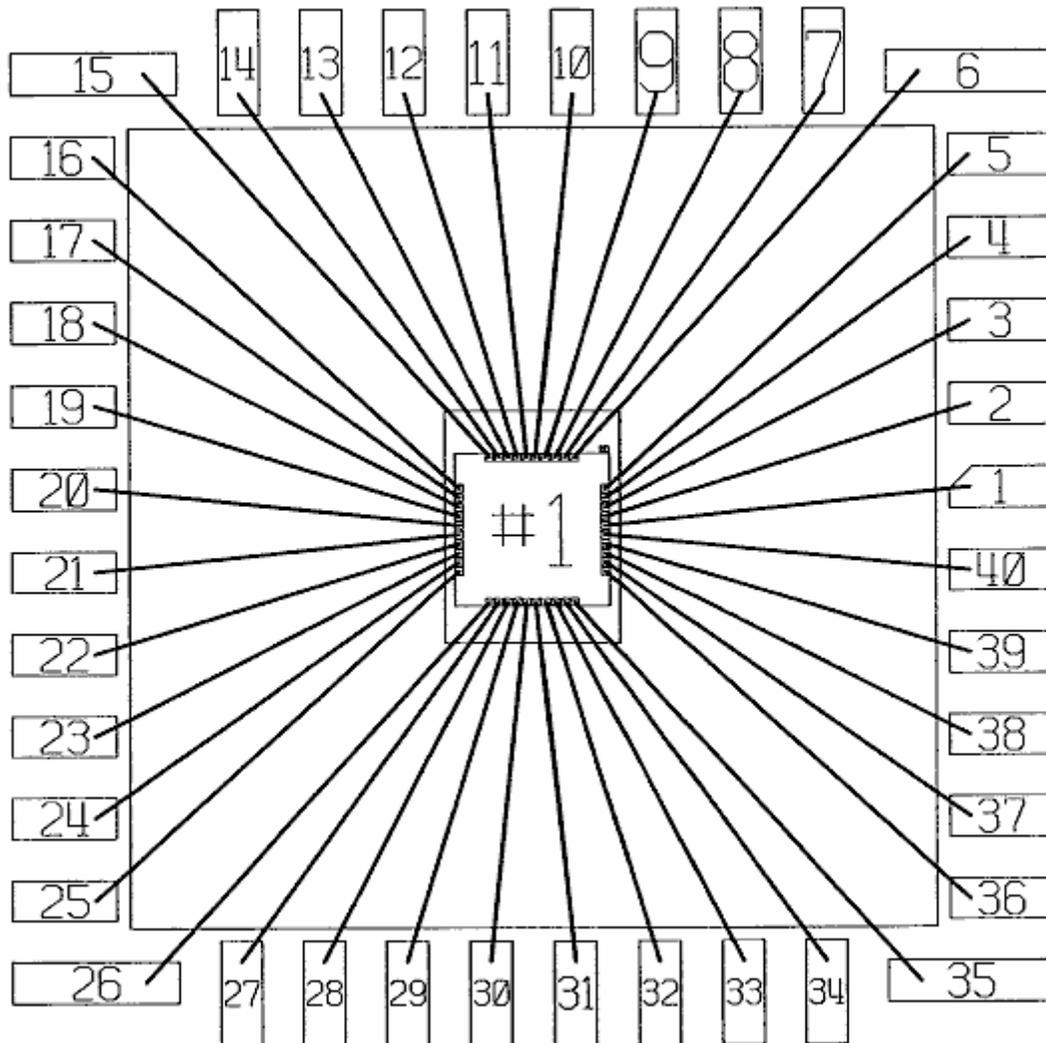
Pad Frame Pin Connections