Thermophysical and Geometrical Effects on the Thermal Performance and Optimization of a Three-Dimensional Integrated Circuit

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A comprehensive analysis and optimization of a three-dimensional integrated circuit (3D IC) structure and its thermophysical attributes are presented in this work. The thermophysical and geometrical attributes studied in this paper include the die, device layer, heat sink, and heat spreader, which are critical structures within a 3D IC. The effect of the power density of the device layer which is the source of heat generation within the chip as well as the through silicon vias (TSV) and microbumps is also considered in our investigation. The thermophysical and geometrical parameters that have a significant impact on the thermal signature of the 3D IC as well as those that have an insignificant impact were established. The comprehensive analysis of different geometrical and thermophysical attributes can guide the design and optimization of a 3D IC structure and decrease the cost. [DOI: 10.1115/1.4033138]

Keywords: thermal management, electronic cooling, 3D IC, heat spreader, heat sink, device layer

Introduction

Three-dimensional integration is emerging as an important technology to improve the computational performance of complementary metal-oxide semiconductor. Thermal issues are recognized to be among the major concerns, which are hindering the widespread adoption of promising 3D ICs. More studies are required to properly establish the thermal characteristics of the 3D ICs. With the development of logic performance, the number of cores is increasing by as much as two times per generation [1]. The z-dimension resources accessibility is highly needed in addition to x- and y-dimensions due to the limitations of two-dimensional connectivity. The design space extends into the third dimension by stacking multiple silicon dies and interconnecting circuits between different dies using TSV. A 3D IC can realize significant electrical performance benefits, such as reducing average wire length, power consumption, and the footprint of the 3D chip [2]. However, 3D IC results in higher power density and heat generation due to the increased integration. Detailed understanding of the thermophysical and geometrical attributes of the heat spreader, heat sink, die, device layer, substrate, power density, and structure of the 3D IC is essential in order to augment and optimize the dissipation of the generated heat efficiently.

Various cooling and thermal management technologies have been developed in the past decades, which can mainly be divided into two main areas. One area is related to convection and conduction cooling enhancement by improving the heat transfer coefficient. The other area is the system-level dynamic thermal management, which uses both hardware and software support to optimize the temperature profile [3].

To increase the heat transfer coefficient, heat spreader and heat sink are a promising solution which should be explored along with other alternatives. A heat spreader is primarily utilized to enlarge the heat dissipating area from the die to the heat sink or the package surface. Several materials are considered for constructing a heat spreader, such as graphene, carbon fiber, graphite, carbon-based composites, synthetic diamonds, and graphite [3]. Carbon-based materials are good options for a heat spreader due to their low density and relatively high thermal conductivity, such as the conductivity of a 2D graphene structure. Different materials and structure of the heat spreader, heat sink, and substrate can significantly affect the heat dissipation from the 3D IC chip.

The structure of the chip, such as the device layer, die and power distribution are also critical factors that substantially impact the thermal profile of the chip. The consideration and analysis of the structure of the 3D IC can help in optimizing its architecture leading to its innovative design fabrication [4]. Optimization of the power distribution or thermal sources can efficiently improve the thermal profile to avoid overheating. Technological optimization includes low power design [5], rearranging the heat source [6], and so on. Low power design can utilize power switches to control power gate and reduce the leakage power. Rearranging the chip structure by physical design (floorplanning and placement) improves the thermal profile and can diminish the hot spot temperatures.

In this work, a comprehensive analysis and optimization of 3D IC structure and its thermophysical attributes are presented. The effect of the die size, device layer, device power, heat spreader, and heat sink is investigated. The effect of TSVs and thermal interface material (TIM) on the above-mentioned areas is also investigated. Furthermore, the geometrical and thermophysical parameters that have significant or insignificant impacts on the thermal attributes of the 3D IC are identified.

Modeling and Analysis

The structure of 3D ICs is typically characterized as stacking layers of circuits, which are linked via interlayer connections. The primary components of a 3D IC include a substrate, die, device

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layer, TIM, heat spreader, and heat sink. The heat generated in each processor is conducted through the circuit layers to the heat spreader and then dissipated to the ambient through the heat sink. The TIM layer can be categorized as microbump TIM layer and C4 bump TIM layer depending on the type of structure utilized in the layer. Our thermal model is based on a generalized 3D IC structure under consideration, based on our nominal structure attributes study. Figure 1 shows the schematic of a nominal 3D IC which was presented in our earlier work [7]. As the schematic illustrates, the structure consists of three circuit layers mounted on the silicon substrate. A TIM is typically utilized between dies or between a die and substrate to minimize the insulating effect of air cavities created at the contact surface of two layers. Thermal grease is usually utilized as TIM due to its adhesive properties and relatively high thermal conductivity. The size of heat spreader and heat sink is usually larger than other layers to increase the surface area exposed to convective cooling and to enhance the overall heat dissipation. In this work, the physics of heat transfer and fluid flow is simulated for steady-state operation of the 3D IC. Heat conduction through the solid and isotropic layers of the 3D IC is governed by

$$\frac{\partial^2 \Theta_s^*}{\partial x^{*2}} + \frac{\partial^2 \Theta_s^*}{\partial y^{*2}} + \frac{\partial^2 \Theta_s^*}{\partial z^{*2}} + \dot{q}_g^* = 0 \tag{1}$$

where $\dot{q}_g^*$ denotes the dimensionless volumetric heat generation in the processors and the nondimensionalized temperature and coordinates are defined as

$$x^* = \frac{x}{H}, \quad y^* = \frac{y}{H}, \quad z^* = \frac{z}{H}, \quad \Theta^* = \frac{T - T_e}{\mathrm{qH}/k_f} \tag{2}$$

The bottom surface of substrate is exposed to natural convection with a nominal convective coefficient of $h_b = 10\,\mathrm{W/(m^2\,K)}$, whereas the top surface of heat sink is cooled by forced convective heat transfer with a nominal convective coefficient $h_t = 400\,\mathrm{W/(m^2\,K)}$ [8,9]. Pertinent aspects related to convective cooling, heat transfer coefficients, extended surfaces, and heat sinks were utilized in our study [10–15]. The convective boundary condition can be represented by

$$\frac{\partial \Theta_s^*}{\partial n} = -Bi \cdot \Theta_s^* \tag{3}$$

where n is the normal coordinate, and Bi is the dimensionless Biot number defined as

$$Bi = \frac{hL_c}{k_s} \tag{4}$$

The continuum fluid flow and heat transfer problems are modeled using the dimensionless Navier–Stokes equations in Cartesian coordinates:

Mass conservation

$$\frac{\partial u^*}{\partial x^*} + \frac{\partial v^*}{\partial y^*} + \frac{\partial w^*}{\partial z^*} = 0 \tag{5}$$

x-momentum conservation

$$\mathrm{Re}_H \left(u^* \frac{\partial u^*}{\partial x^*} + v^* \frac{\partial u^*}{\partial y^*} + w^* \frac{\partial u^*}{\partial z^*} \right) = -\frac{\partial p^*}{\partial x^*} + \left(\frac{\partial^2 u^*}{\partial x^{*2}} + \frac{\partial^2 u^*}{\partial y^{*2}} + \frac{\partial^2 u^*}{\partial z^{*2}} \right) \tag{6}$$

y-momentum conservation

$$\mathrm{Re}_H \left(u^* \frac{\partial v^*}{\partial x^*} + v^* \frac{\partial v^*}{\partial y^*} + w^* \frac{\partial v^*}{\partial z^*} \right) = -\frac{\partial p^*}{\partial y^*} + \left(\frac{\partial^2 v^*}{\partial x^{*2}} + \frac{\partial^2 v^*}{\partial y^{*2}} + \frac{\partial^2 v^*}{\partial z^{*2}} \right) \tag{7}$$

z-momentum conservation

$$\mathrm{Re}_H \left(u^* \frac{\partial w^*}{\partial x^*} + v^* \frac{\partial w^*}{\partial y^*} + w^* \frac{\partial w^*}{\partial z^*} \right) = -\frac{\partial p^*}{\partial z^*} + \left(\frac{\partial^2 w^*}{\partial x^{*2}} + \frac{\partial^2 w^*}{\partial y^{*2}} + \frac{\partial^2 w^*}{\partial z^{*2}} \right) \tag{8}$$

Energy conservation for the fluid domain

$$Pe_H \left(u^* \frac{\partial \Theta_f^*}{\partial x^*} + v^* \frac{\partial \Theta_f^*}{\partial y^*} + w^* \frac{\partial \Theta_f^*}{\partial z^*} \right) = \frac{\partial^2 \Theta_f^*}{\partial x^{*2}} + \frac{\partial^2 \Theta_f^*}{\partial y^{*2}} + \frac{\partial^2 \Theta_f^*}{\partial z^{*2}} \tag{9}$$

The governing equations were nondimensionalized using the following equation:

$$u^* = \frac{u}{u_m}, \quad v^* = \frac{v}{u_m}, \quad w^* = \frac{w}{u_m}, \quad p^* = \frac{\mathrm{pH}}{\mu_f u_m}, \quad Re_H = \frac{\rho_f u_m H}{\mu_f}, \quad Pe_H = \frac{\rho_f c_{p,f} u_m H}{k_f} \tag{10}$$

The nominal thermal power for each processing unit is $p = 7.5\,\mathrm{W}$ per processor, which results in a total power of $P = 30\,\mathrm{W}$ per layer. Therefore, the total power consumption for a three layer

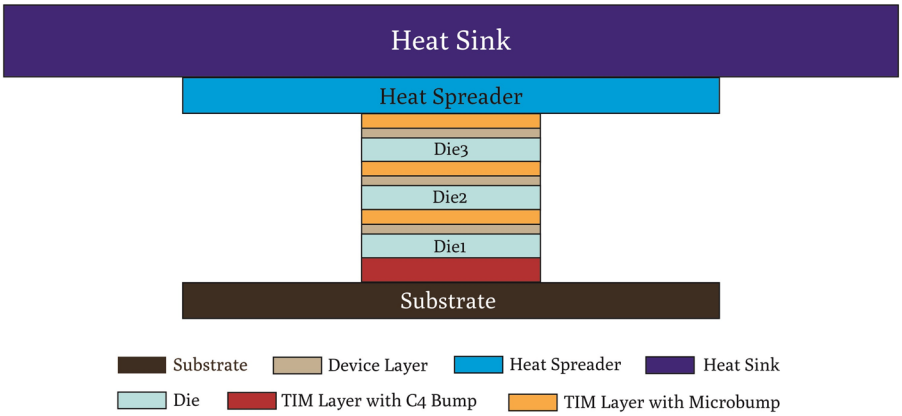

Fig. 1 Schematic of the 3D IC [7]

nominal 3D IC chip is $P = 90W$. The 3D IC experiences an incoming air flow at ambient temperature with Reynolds number of $\mathrm{Re} = 1500$, where the characteristic length is the height of the 3D IC package excluding the heat sink. At the channel outlet, the cooling fluid is assumed to exit the package at atmospheric pressure with negligible streamwise temperature gradient. The outlet boundary conditions are as follows:

$$p_o = 1\ \text{atm}, \quad \frac{\partial \Theta_f^*}{\partial x^*} = 0 \tag{11}$$

Table 1 presents the nominal values for various components of the 3D IC, such as material selection, dimensional attributes, and number of layers, based on the pertinent thermal analysis of 3D ICs performed in previous work [7]. The nominal values for different geometrical and thermophysical attributes of TSVs utilized in the 3D IC structure, based on values obtained from pertinent literature, are also given in Table 1. TSVs are classified into three types: power, signal, and thermal TSVs, where power and signal TSVs act as electrical and signal interconnection between device layers, while thermal TSVs are used to enhance heat conduction through various layers of the 3D IC.

As there are TSVs and bumps within the dies and TIM layers, the effective thermal conductivity needs to be determined for each layer. The effective thermal conductivity can be determined by a method proposed by Tien and Vafai [16]. Based on their analysis, the effective thermal conductivity satisfies the following inequality:

$$A \le \frac{k_e}{\sqrt{k_1 k_2}} \le B \tag{12}$$

where

$$A = \sqrt{\beta}\left\{\beta - \delta_V(\beta-1) - \frac{(1-\beta)^2\delta_V(1-\delta_V)}{2(1-\beta)\delta_V + 2\beta + 4(\beta-1)(2\delta_V-1)G}\right\}^{-1} \tag{13}$$

$$B = \frac{1+\delta_V(\beta-1)}{\sqrt{\beta}} \times \left\{1 - \frac{\left[\delta_V(1-\delta_V)(\beta-1)^2\right]}{2[1+\delta_V(\beta-1)]\left[1+(\beta-1)\delta_V + 2(\beta-1)(1-2\delta_V)G\right]}\right\} \tag{14}$$

β denotes the thermal conductivity ratio of two components ($\beta = k_1/k_2$), and δ_V represents the volume fraction of the component with thermal conductivity of k_1. The mean value of the inequality represented by $k_e/\sqrt{k_1 k_2} = A + B/2$ is used as the effective thermal conductivity of medium.

The COMSOL MULTIPHYSICS simulation tool has been used to set up our thermal models. Two sets of comparisons are employed to verify the accuracy of our models. One is the comparison with an analytical solution. The other comparison is with the numerical results of Young and Vafai's work[17]. Both of these comparisons were established earlier displaying very close results as shown in Ref. [7].

Table 1 Nominal values for different parameters within the 3D IC structure [7]

Component	Property	Nominal value
Chip	Area	$10 \times 10\ \text{mm}^2$
	Number of layers	3
CPU	Area	$1 \times 1\ \text{mm}^2$
	Thickness	$2\ \mu$m
	Material	Silicon
	Number of cores within each layer	4
	Total thermal power	90
Heat sink	Area	$50 \times 50\ \text{mm}^2$
	Thickness	4 mm
	Material	Copper
Heat spreader	Area	$30 \times 30\ \text{mm}^2$
	Thickness	2 mm
	Material	Copper
Thermal TSV	Diameter	$100\ \mu$m
	Number	5
	Material	Copper
Power TSV	Diameter	$20\ \mu$m
	Number	400
	Material	Copper
Signal TSV	Diameter	$10\ \mu$m
	Number	4×10^4
	Material	Copper
TIM with microbump	Thickness	$15\ \mu$m
	Thermal conductivity	5 W/m K
	Material	Thermal grease
TIM with C4 bump	Thickness	$100\ \mu$m
	Thermal conductivity	5 W/m K
	Material	Thermal grease
Device layer	Thickness	$2\ \mu$m
	Material	Silicon
Die	Thickness	$100\ \mu$m
	Material	Silicon
Substrate	Area	$30 \times 30\ \text{mm}^2$
	Thickness	1 mm
	Material	Silicon

Results and Discussion

Figure 2 shows the temperature profile for the entire 3D IC for the nominal case. It can be seen that the temperature in the front edge of the incoming air flow has the lowest value because the air temperature is lower at this point before it is heated as it moves through the chip existing from the back end. The hotspot (maximum) temperature, which is about 350 K in the nominal case, occurs within the core processing units (CPUs) as they are the primary source of heat generation. The bottom device layer is the layer close to the substrate, and the top device layer is close to the heat spreader. It is found that the bottom device layer, farthest from heat sink, has the highest temperature compared to the other device layers, while the top device layer, closest to heat sink, has the lowest temperature. This is due to the fact that heat sink provides a better path way for dissipating the heat from the upper device layers. That is, the top device layer is closer to the heat sink, which dissipates the generated heat from the circuit.

In the current work, the effect of the number of dies and their sizes, device layer sizes and thicknesses, heat spreader and heat

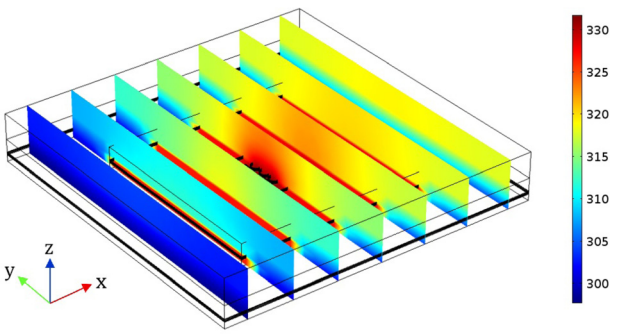

Fig. 2 Temperature distribution of the nominal 3D IC structure

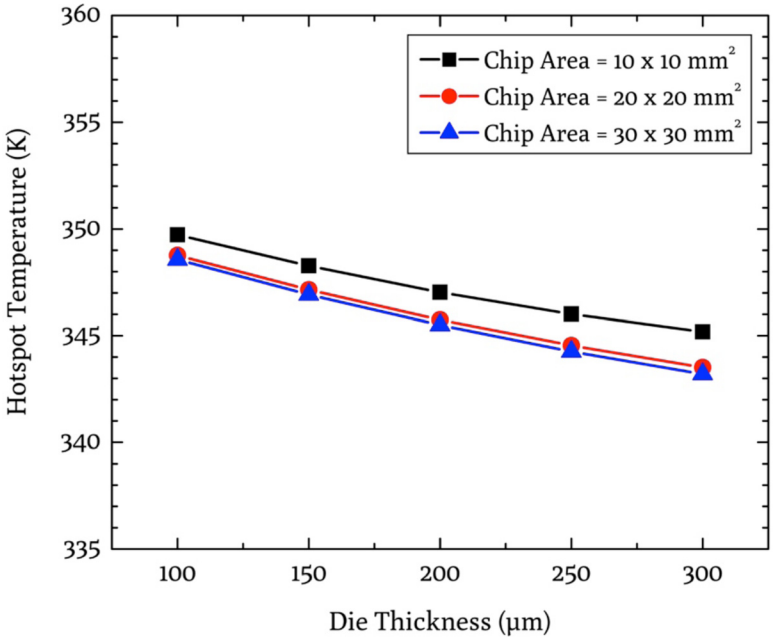

Fig. 3 Effect of thickness of the die and area of the chip on the hotspot temperature

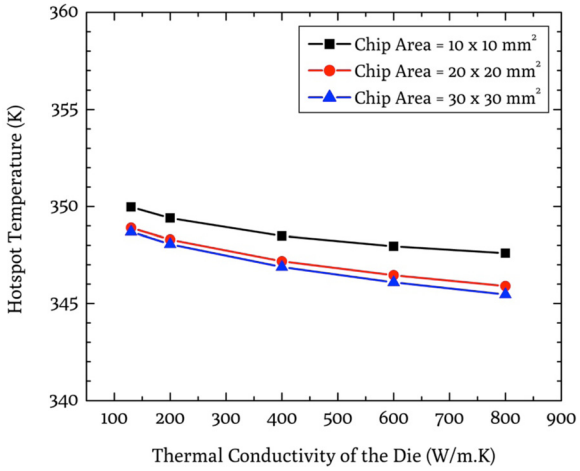

Fig. 4 Effect of thermal conductivity of the die and area of the chip on the hotspot temperature

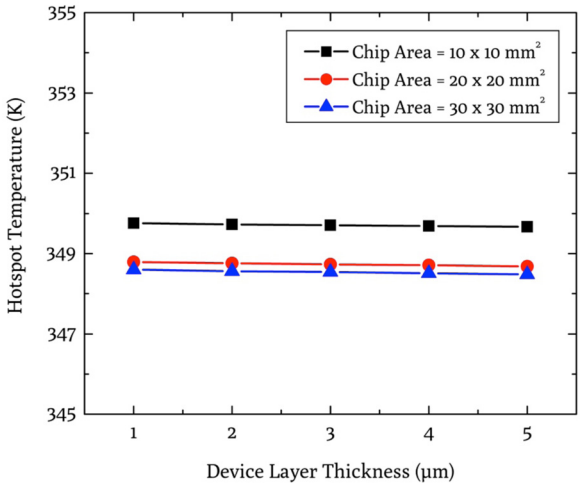

Fig. 5 Effect of thickness of the device layer and area of the chip on the hotspot temperature

sink sizes and thicknesses, thermophysical properties, and device power is analyzed.

Three different chip areas are selected for evaluating the effect of chip size on thermal performance. The areas (width and depth) are 10 mm × 10 mm, 20 mm × 20 mm, and 30 mm × 30 mm, respectively. For these three cases, the thermal power for each device layer is set to $p = 30$ W. Figure 3 shows the effect of the die thickness on the hot spot temperature for different chip areas for the 3D IC model. Since the bottom device layer is the hottest, the results shown in Fig. 3 reflect the highest temperature values for this layer. The highest temperatures for these three cases are 350 K, 349 K, and 348.5 K, respectively.

More dies can translate into more cores resulting in a possible improvement in the computing performance. There has been a speculation that if one can overcome the manufacturing difficulty when increasing the number of dies can possibly alleviate some of the thermal issues. As such, Fig. 4 presents the effect of an increase in the die thickness representing an increase in the number of dies. A range of die thicknesses from 100μm to 300μm were considered. Figure 3 shows that an increase in the number of dies from the nominal case has a relatively insignificant effect on the hot spot temperatures.

Figure 4 shows the effect of the thermal conductivity of the die on the hot spot temperature. As it can be seen, the variations in the thermal conductivity of the die also have a relatively insignificant effect on the hot spot temperatures.

The effect of the device layer thickness is investigated in Fig. 5. Figure 5 presents a range of variation of the device layer from 1μm to 5μm for three different chip areas. The power for each layer is kept at $p = 30$ W for all the cases. Figure 5 shows that the device layer thickness has a minimal effect on the highest temperatures. This means that for the same power density, the transistor placement at different thicknesses will not affect the highest temperature.

The effect of the TIM layer thickness on the hot spot temperatures for different chip layers is shown in Fig. 6. As it can be seen,

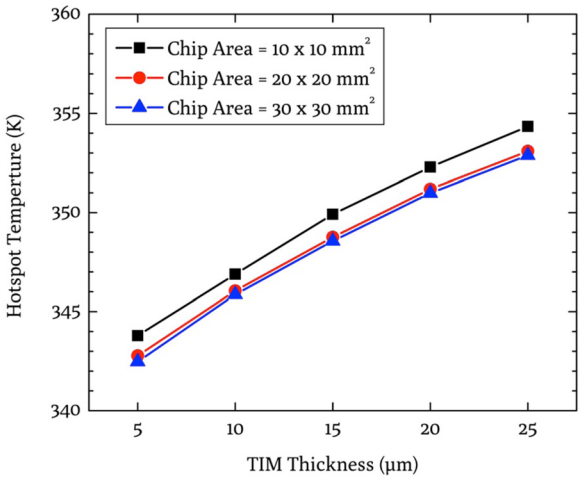

Fig. 6 Effect of thickness of the TIM and area of the chip on the hotspot temperature

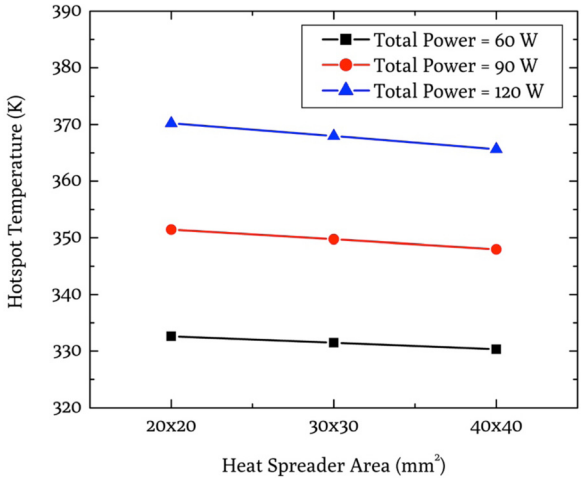

Fig. 8 Effect of area of the heat spreader and total thermal power of the chip on the hotspot temperature

the TIM layer thickness has a significant effect on the hot spot temperature.

The use of heat spreader can improve the heat dissipation and heat transfer coefficient. The selection of material for the heat spreader will directly affect the temperature distribution in the chip. For the same heat flux, the higher thermal conductivity translates into a lower temperature difference between the heat sink and the midsection of the chip. A range of thermal conductivities representing different materials, such as aluminum, copper, and composite materials, are selected for comparison. Also, the effect of the thickness and size of the heat spreader is analyzed. These results are displayed in Figs. 7 and 8. In addition, the impact of the total power on the hot spot temperatures for different size 3D chips is shown in Fig. 8. As it can be seen, the thermal conductivity of the heat spreader has a significant impact in reducing the hot spot temperatures, while the size of the heat spreader has a minimal effect.

The thickness of the heat sink is also an important factor for the heat dissipation. As can be seen in Fig. 1, the heat spreader and heat sink take up a substantial portion of the 3D IC space. The heat sink thickness affects the temperature profile as seen in Fig. 9. As can be seen, a thinner heat sink resulting in a thinner chip structure can have a substantially adverse impact in terms of the hot spot temperatures. Three thicknesses of the heat sink were considered here. These were 2 mm, 4 mm, and 6 mm. The nominal

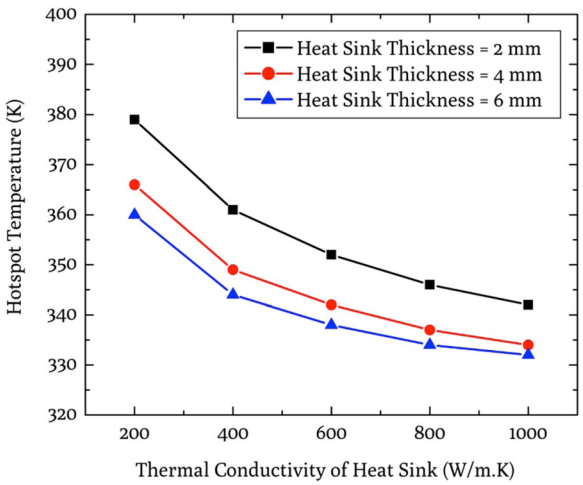

Fig. 9 Effect of thermal conductivity and thickness of the heat sink on the hotspot temperature

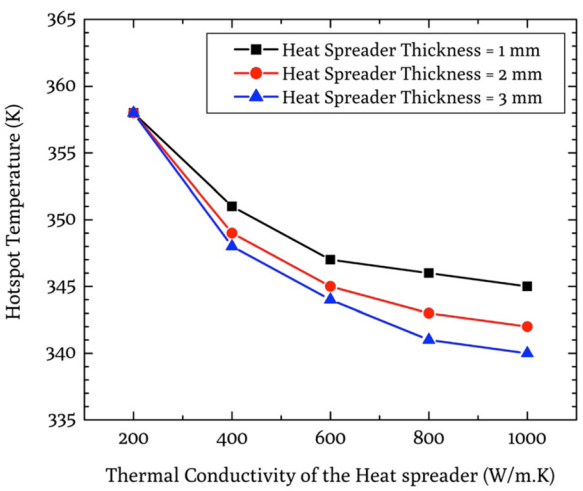

Fig. 7 Effect of thermal conductivity and thickness of the heat spreader on the hotspot temperature

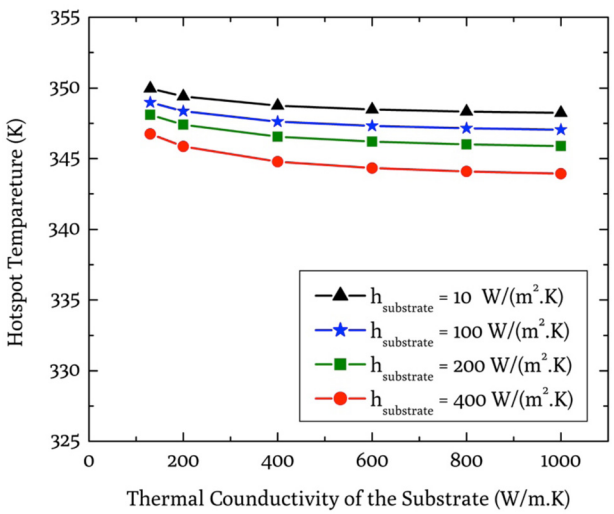

Fig. 10 Effect of thermal conductivity and convective heat transfer coefficient of the substrate on the hotspot temperature

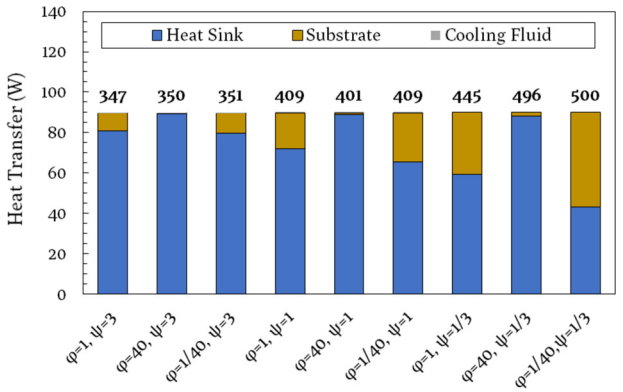

Fig. 11 Effect of the ratio of the heat sink to substrate convective heat transfer coefficient (ϕ) and thermal conductivity (ψ) on heat dissipation within the 3D IC chip and the hotspot temperatures

material for the heat sink is copper. However, in Fig. 9 a range of different materials were also chosen to display the impact of variations in thermal and geometrical attributes of the heat sink on the temperature signature of the 3D chip. For the nominal case, the temperature decreases by 12 K when the thickness increases from 2 mm to 4 mm and when the thickness increases from 4 mm to 6 mm, the temperature decreases by another 5 K. So when a smaller size chip is desired, decreasing the thickness of the heat sink is not an attractive alternative. The impact of the use of different materials for the substrate is shown in Fig. 10. As it can be seen, the substrate material has a minimal impact on the hotspot temperature.

One interesting aspect, which was found through our analysis, was related to the ratio of heat dissipation from the heat sink at the top of the 3D IC to that of the substrate, which is at the bottom. In this figure, effect of the ratio of the heat sink to substrate convective heat transfer coefficient (ϕ) and thermal conductivity (ψ) on heat dissipation within the 3D IC chip and the hotspot temperatures is displayed. As can be clearly seen in Fig. 11, substantially more of the generated heat from the CPU's escapes through the heat sink as compared to the substrate.

Conclusions

A comprehensive analysis and optimization of the thermophysical and geometrical attributes including the die, device layer, substrate, heat sink, and heat spreader, which are critical structures within a 3D IC, were presented in this study. The effect of the power density of the device layer as well as the TSV and microbumps was considered in this investigation. The geometrical and thermophysical parameters that have an insignificant impact on the thermal attributes of the 3D IC as well as those that have a significant impact were established. It was shown that the die and device layer thicknesses, thermal conductivity of the die, and the substrate and the heat spreader area have an insignificant effect on the thermal signature of the chip. On the other hand, the thermal conductivities of the heat spreader and heat sink and the TIM and heat spreader thicknesses have a substantial impact on the thermal profile of the 3D IC. The comprehensive analysis of different geometrical and thermophysical attributes will provide the required guidelines for the design and optimization of a 3D IC structure in order to decrease the cost.

Nomenclature

c_p = specific heat at constant pressure (J $(\text{kg K})^{-1}$)
G = cell geometric factor
h = convective heat transfer coefficient (W $(\text{m}^2\,\text{K})^{-1}$)
H = height (m)
k = thermal conductivity (W $(\text{m K})^{-1}$)
L = length (m)
L_c = characteristic length (m)
n = normal coordinate
N = system dimension
p = pressure (Pa)
Pe_H = Péclet number ($\rho_f c_{p,f} u_m H/k_f$)
q = heat flux (W m^{-2})
$\dot{q}_g$ = volumetric heat generation rate (W m^{-3})
Re_H = Reynolds number ($\rho_f u_m H/\mu_f$)
T = temperature (K)
u = x-component of velocity (m s^{-1})
v = y-component of velocity (m s^{-1})
w = z-component of velocity (m s^{-1})
x, y, z = Cartesian coordinates

Greek Symbols

β = thermal conductivity ratio (k_1/k_2)
δ_V = volume fraction
Θ = dimensionless temperature $[(T - T_e)/(q''H/k_f)]$
μ = dynamic viscosity $((\text{N s})\text{m}^{-2})$
ρ = density (kg m^{-3})
ϕ = ratio of heat sink to substrate convective heat transfer coefficient $[h_t/h_b]$
ψ = ratio of heat sink to substrate thermal conductivity $[k_t/k_b]$

Subscripts

b = bottom surface (substrate)
e = entrance
f = fluid
m = mean
o = outlet
s = solid
t = top surface (heat sink)
w = wall
ε = effective
0 = initial

Superscript

* = dimensionless

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