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Analysis of critical thermal issues in 3D integrated circuits

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ABSTRACT

Several key attributes of a 3D integrated chip structure are analyzed in this work. Critical features related to the effect of the size of the substrate, heat sink, device layer, through silicon vias (TSVs), thermal interface material (TIM), and the pitch and arrangement of core processors and TSVs as well as variation of thermal conductivity and total heat dissipation and distribution of power within the device layers core processors are investigated in depth. The effects of variation of pertinent features of the 3D integrated circuit (IC) structure on thermal hotspots are established and an optimization route for its reduction is clarified. In addition, a revealing analysis that shows the effect of the number of layers in the 3D structure is presented. Furthermore, the features that have insufficient effect on reduction of thermal hotspots are also established and discussed.

1. Introduction

The existing integrated circuit technology is not sufficient to fulfill the requirements of future electronic systems including portable communication devices (such as laptops, smart phones, smart watches, etc.) that need reliable combination of numerous subsystems (e.g. sensors, actuators, memory, etc.) and highly efficient processing capabilities while requiring minimum footprint and power consumption. The current technology, so-called embedded systems, is not only too costly and complicated, but also require substantial quantity of connections resulting in reduced performance and increased power consumption [1]. Three-dimensional (3D) integration has been proposed, as a promising solution for future needs of miniaturized systems. A 3D integrated circuit is fabricated by assembling multiple electronic chips and subsequently connecting them with through-silicon vias (TSVs) such that the entire system performs as an integrated device. 3D IC offers superior performance compared to conventional 2D technology since the functional blocks of its structure are closer and localized resulting in greater quantity of accessible neighbors and higher bandwidth. In addition, the shorter interconnects and consequently reduced capacitance, not only decrease the total active power significantly, but also minimize the noise due to synchronous switching events. Other benefits include higher package density, condensed footprint and enhanced functionality [2].

Thermal management is the key issue in developing future generations of integrated systems as chip density and clock speed are continuously increasing. Thermal characteristics will greatly influence design, performance, and reliability of advanced circuit architectures [3]. Thermal management is already a critical issue in 2D IC technology due to the poor thermal conductivity of dielectric materials causing thermal hotspots and consequently overall performance discrepancy. It has been shown that every 10 °C increase in junction temperature results in 1.2% deterioration in the clock buffer performance, indicating the importance of minimizing thermal hotspots in electronic circuits [2,4].

Thermal management of 3D ICs is even more challenging due to higher power density and lower surface-to-volume ratio of 3D structures. Hence, thermal hotspots in 3D ICs can accelerate failure mechanisms such as junction leakage and electromigration, resulting in degradation of device performance and reduction in reliability and lifetime of the integrated system [5]. Therefore, thermal analysis of 3D ICs is essential not only to understand the limits of this technology, but also to find the optimum design characteristics such that thermal hotspots are minimized.

Several techniques have been proposed to address the thermal issues of 3D ICs including task scheduling, floor planning, advanced materials (e.g. carbon nanotube, graphene) and novel cooling technologies (e.g. heat pipes, microchannels) [6]. Task scheduling algorithms attempt to balance the power consumption of cores and optimize the supply voltage through software-hardware cooperation in order to minimize the peak temperature while accomplishing each processing task on time [7–9]. On the other hand, Floor planning is a design-stage optimization method used

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Nomenclature

c_p	specific heat at constant pressure [J (kg·K)$^{-1}$]
D_h	hydraulic diameter [m]
G	cell geometric factor
h	convective heat transfer coefficient [W (m^2·K)$^{-1}$]
H	height [m]
k	thermal conductivity [W (m·K)$^{-1}$]
L	length [m]
L_c	characteristic length [m]
n	normal coordinate
N	system dimension
Nu	Nusselt number [$h \cdot H/k_f$]
p	pressure [Pa]
Pe_H	Péclet Number [$\rho_f c_{p,f} u_m H/k_f$]
Pr	Prandtl number [$\mu_f c_{p,f}/k_f$]
q	heat flux [W m^{-2}]
$\dot{q}_g$	volumetric heat generation rate [W m^{-3}]
Re_H	Reynolds number [$\rho_f u_m H/\mu_f$]
T	temperature [K]
u	x-component of velocity [m s^{-1}]
v	y-component of velocity [m s^{-1}]
w	z-component of velocity [m s^{-1}]
x, y, z	Cartesian coordinates

Greek symbols

β	thermal conductivity ratio [k_1/k_2]
μ	dynamic viscosity [(N·s) m^{-2}]
Θ	dimensionless temperature [$(T - T_e)/(q'' H/k_f)$]
ρ	density [kg m^{-3}]
δ_V	volume fraction

Subscripts

f	fluid
e	entrance
ε	effective
m	mean
o	outlet
s	solid
w	wall
0	initial

Superscript

*	dimensionless

to compromise between performance, temperature, and power consumption in a way that thermal hotspots are positioned far apart, while regularly interacting functional units are closer [10–13].

Thermal issues of 3D ICs must be considered from the initial phases of chip designing, as various parameters including the number and position of cores will affect power and thermal performance. Therefore, it is essential to perform detailed thermal analysis at the design stage in order to implement the most effective thermal management techniques [14]. Amongst the initial attempts for establishing thorough understanding of thermal performance of miniaturized electronic systems, Young and Vafai [15–17] conducted a detailed and extensive analysis of convective flow and heat transfer within an enclosure with two-dimensional array of heated obstacles. Their results showed that flow and heat transfer characteristics can be passively enhanced through proper selection of size, shape, and position of obstacles. Mahjoob and Vafai [18,19] also studied thermal management for electronic applications and showed that prescribing appropriate pertinent parameters result in optimized thermal characteristics.

In this study, we perform a comprehensive thermal analysis of 3-D high performance chips using numerical simulations in order to establish a set of guidelines to be considered by chip architects

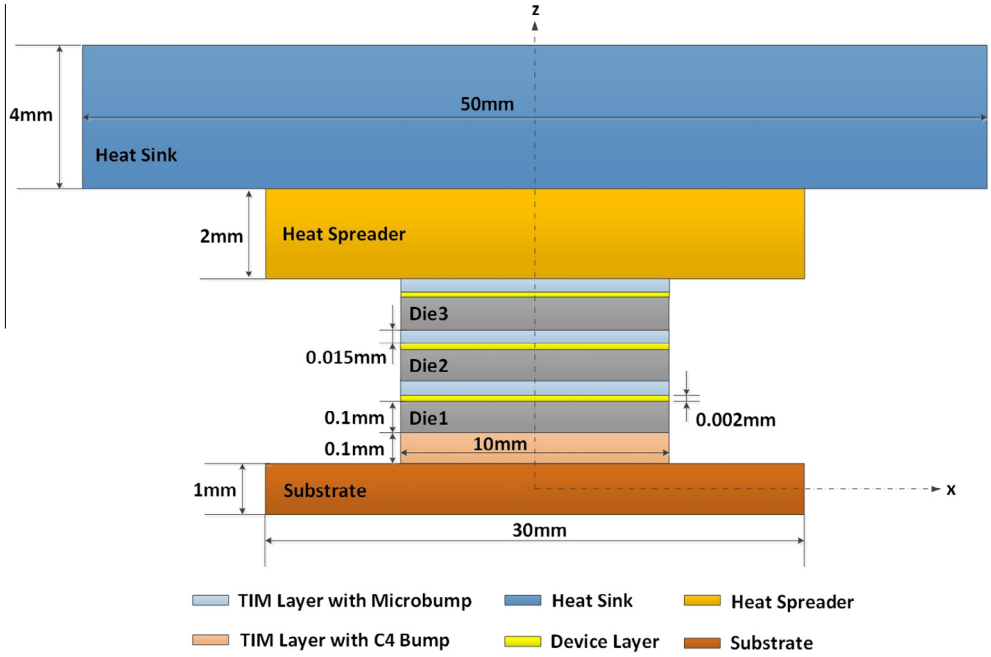

Fig. 1. Schematic of the nominal 3D IC structure.

Table 1
Nominal values and the range of variations for various parameters within the 3D IC structure.

Layer	Parameter	Range	Nominal Value	Unit	References
Heat sink	Material	Cu, Al	Cu	–	[25–27]
	Length & width	20–70	50	mm	[25–27]
	Thickness	2–5	4	mm	[25–27]
Heat spreader	Material	Cu	Cu	–	[25,26,28]
	Length & width	28–40	30	mm	[25,26,28]
	Thickness	1–2.25	2	mm	[25,26,28]
Chip	Length & width	5–25	10	mm	[28–35]
	Number of layers	2–4	3		[30,28,35,36]
TIM layer with microbump	TIM material	Thermal grease	Thermal grease	–	[25,26,33–35,37–39]
	Thermal conductivity	0.2–15	5	$W\,(m{\cdot}K)^{-1}$	[25,26,33–35,37–39]
	Thickness	10–50	15	μm	[25,26,33–35,37–39]
TIM layer with C4 bump	Material	Thermal grease	Thermal grease	–	[25,26,33–35,37–39]
	Thermal conductivity	0.2–15	5	$W\,(m{\cdot}K)^{-1}$	[25,26,33–35,37–39]
	Thickness	25–150	100	μm	[25,26,33–35,37–39]
Die	Material	Si	Si	–	[26,30,34,39]
	Thickness	100–500	100	μm	[30,28,32,35]
Device layer	Material	Si	Si	–	[28,30,34,39]
	Thickness	1–5	2	μm	[28,30,34,39]
Core processor	Material	Si	Si	–	[25,26,29–32,34,39]
	Total power within the 3D IC	10–250	90	W	[25,26,29–32,34,39]
	Cores per layer	1–8	4	–	[8,9,26,28,29]
	Length & width	0.2–3	1	mm	[8,9,26,28,29]
	Thickness	2–10	2	μm	[8,9,26,28,29]
Substrate	Material	Si, AlN	Si	–	[32–34,37]
	Length & width	2.5–45	30	mm	[32–34,37]
	Thickness	0.05–1.6	1	mm	[32–34,37]

for designing new generation of 3D integrated circuits with optimized thermal performance. A 3D IC structure with nominal thermophysical properties and dimensional attributes, based on available pertinent literature, is used as the baseline for conducting the analysis. The effect of parametric changes in the geometrical configuration, such as size, number and spacing, as well as thermophysical properties of the chip and cooling fluid, on the flow and heat transfer is investigated through perturbing the baseline case in order to develop key thermal management attributes. In addition, the dependence of thermal hotspots as well as thermal attributes on the alteration of pertinent parameters such as the size of device layers, heat sink, substrate, TIM, TSV, the pitch, power distribution within the core processors, and the material selection is documented for establishing the essential principles for optimizing the overall thermal performance. Furthermore, the geometrical and thermophysical features with insignificant impact on thermal characteristics are also established and discussed. The results presented here provide the key features to be used for establishing optimized design and setup of 3D ICs as well as the pathway for future studies in this area.

Table 2
Nominal values and the range of variations for various parameters for TSVs and bumps within the 3D IC structure.

Layers	Parameters	Range	Nominal Value	Units	Reference
Power TSV	Material	Cu	Cu	–	[1,35,40,41]
	Diameter	1–60	20	μm	[1,35,40,41]
	Pitch	0.5–10	5	μm	[1,35,40,41]
Signal TSV	Material	Cu	Cu	–	[1,35,40,41]
	Diameter	1–20	10	μm	[1,35,40,41]
	Pitch	0.5–20	10	μm	[1,35,40,41]
Thermal TSV	Material	Cu	Cu	–	[29,33,34,39]
	Diameter	10–250	100	μm	[29,33,34,39]
	Pitch	0.2–2	1	mm	[29,33,34,39]
C4 bump	Material	SnAg, SnAgCu	SnAgCu	–	[31–34]
	Diameter	50–200	100	μm	[31–34]
	Pitch	150–250	200	μm	[31–34]
Microbump 1	Material	SnAg, Cu	Cu	–	[26,32,34,41]
	Diameter	2–20	15	μm	[26,32,34,41]
	Pitch	5–40	20	μm	[26,32,34,41]
Microbump 2	Material	Cu	Cu	–	[26,32,34,41]
	Diameter	20–70	45	μm	[26,32,34,41]
	Pitch	5–100	50	μm	[26,32,34,41]

2. Modeling and analysis

In this work, based on our nominal study to be presented later, the thermal analysis of a 3D chip with multiple active silicon layers is performed. Thermal and flow characteristics are investigated and the temperature distribution and heat flux across the chip are studied through numerical modeling of a generalized geometry of 3D IC with properly specified boundary conditions. The structure of 3D ICs is typically categorized based on the design of stacked circuit layers. For clarity in our analysis, the 3D IC is characterized as stacking layers of circuits, chips, and devices. The heat generated in each CPU due to transistor switching, is conducted through the layers to the package and then dissipated to the ambient via convective heat transfer. It should be noted that the rate of heat conduction can be very small in some layers as the device layers are electrically insulated from each other via dielectric materials that typically have substantially lower thermal conductivity compared to silicon [5].

Fig. 1 shows the schematic of the generalized 3D IC structure under consideration, based on our nominal structure attributes study, which incorporates substrate, thermal interface material (TIM), die, device layer, heat spreader, and heat sink. As the schematic illustrates, the device layers are bonded between TIM layer and silicon die where each device layer comprises various electronic subsystems including processor, memory, sensor, etc. Since the processor is the primary functional unit that dissipates a

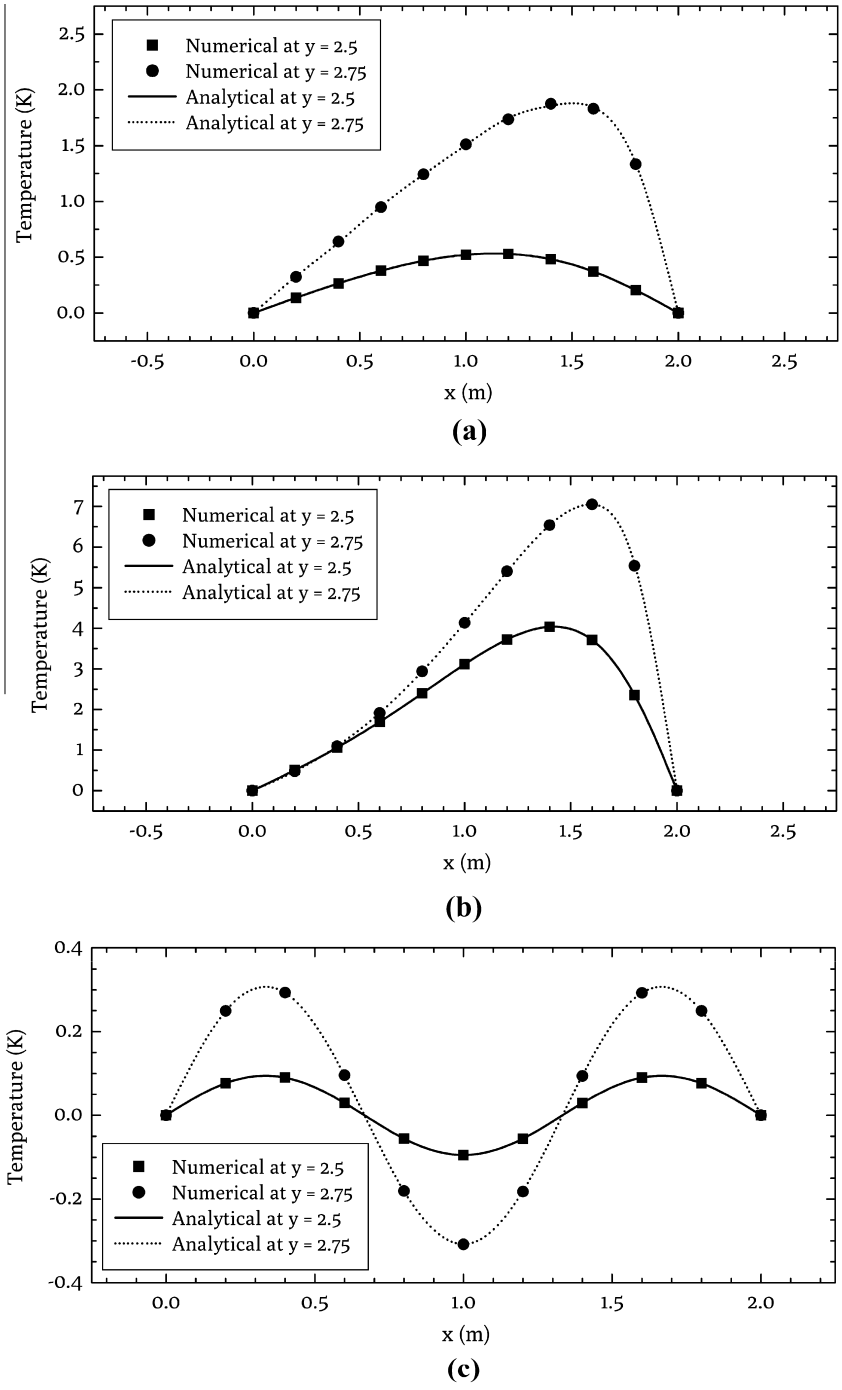

Fig. 2. Comparison with an analytical solution for a slab (a) $f(x) = 2x$, (b) $f(x) = 5x^2$, (c) $f(x) = \sin\left(\frac{3\pi x}{L}\right)$.

significant fraction of heat, the effect of other units is considered to be negligible in this study. The thermal interface material is used in order to enhance conductive heat transfer between the device layers and the die so that the insulating effect of air cavities created at the contact surface of two solid layers is minimized. Based on the pertinent literature for the nominal study, TIM layer comprised of C4 bumps is used to connect the silicon substrate and the die closest to it, while micro-bump TIM layers are utilized for bonding the device layers with the layer above it. The size of heat spreader and heat sink are typically larger than other layers in order to extend the surface area exposed to the cooling fluid and consequently to enhance the heat transfer to the ambient fluid.

In this study, heat transfer and fluid flow physics are modeled for steady state operation of the 3D IC. Conductive heat transfer through the solid, and isotropic layers of the IC are governed by

$$\frac{\partial^2 \Theta_s^*}{\partial x^{*2}} + \frac{\partial^2 \Theta_s^*}{\partial y^{*2}} + \frac{\partial^2 \Theta_s^*}{\partial z^{*2}} + \dot{q}_g^* = 0 \tag{1}$$

where $\dot{q}_g^*$ represents the dimensionless volumetric heat generation in the central processing units (CPUs) and the nondimensionalized temperature and coordinates are defined as:

$$x^* = \frac{x}{H}, \quad y^* = \frac{y}{H}, \quad z^* = \frac{z}{H}, \quad \Theta^* = \frac{T - T_e}{qH/k_f} \tag{2}$$

Table 3
Nominal effective thermal conductivity of various layers [W (m·K)$^{-1}$].

Layer	Maxwell Garnett	Tien and Vafai
Die with uniformly distributed TSVs	5.7	6.3
TIM layer with microbump	7.9	7.2
TIM layer with C4 bump	135	135

General features of the 3D IC are such that the lateral sides of the chip are exposed to variable air speed cooling and the bottom surface of substrate is cooled by natural convection with general convective coefficient of h_b while the top surface of heat sink is exposed to forced convective heat transfer with variable spatial convective coefficient h_t. The convective boundary condition can be represented by:

$$\frac{\partial \Theta_s^*}{\partial n} = -\mathrm{Bi} \cdot \Theta_s^* \tag{3}$$

where n is the normal coordinate and Bi is the dimensionless Biot number defined as:

$$\mathrm{Bi} = \frac{hL_c}{k_s} \tag{4}$$

The continuum fluid flow and heat transfer problems are modeled using the dimensionless Navier–Stokes equations in Cartesian coordinates:

Mass conservation:

$$\frac{\partial u^*}{\partial x^*} + \frac{\partial v^*}{\partial y^*} + \frac{\partial w^*}{\partial z^*} = 0 \tag{5}$$

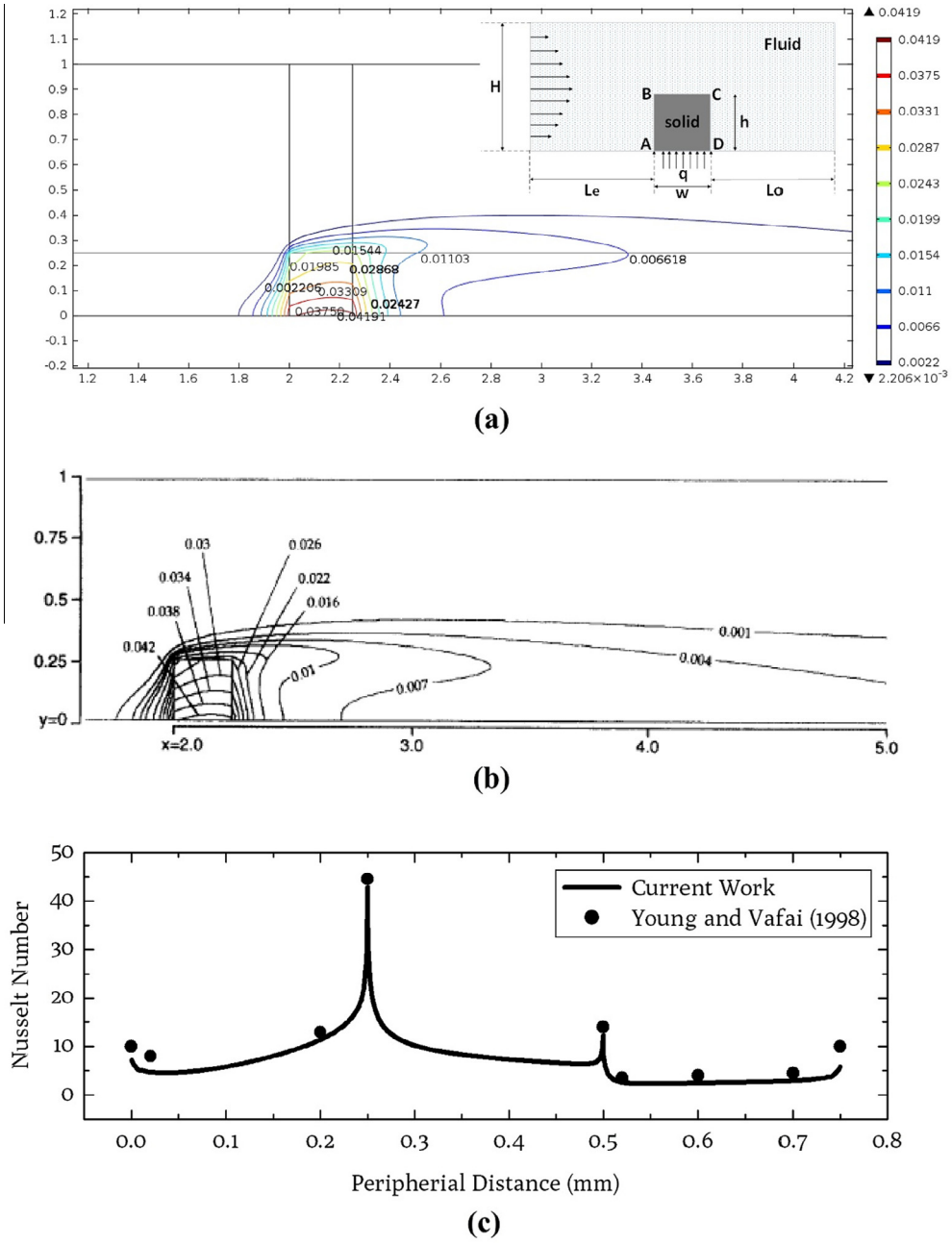

Fig. 3. Comparison with Young and Vafai's [16] work (a) dimensionless temperature contour in our simulation (b) dimensionless temperature contour from Young and Vafai's work (c) local Nusselt number distribution around the three exposed faces of the obstacle compared with Young and Vafai's [16] work.

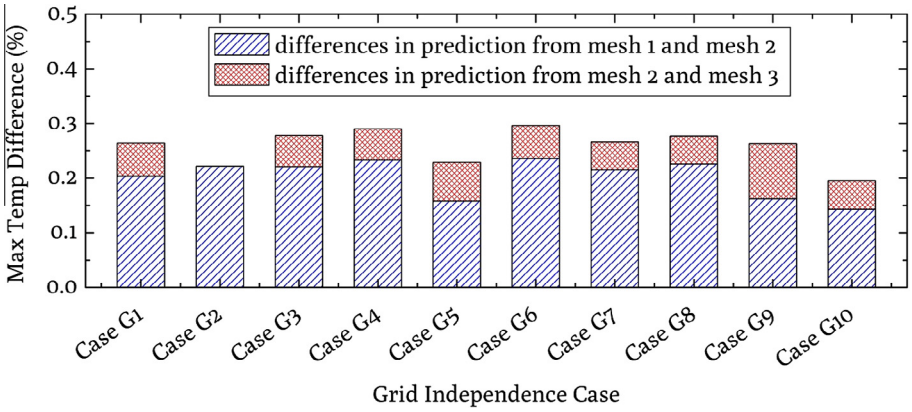

Fig. 4. Grid independence study: the coarsest mesh (mesh 1), finer mesh (mesh 2), and the finest mesh (mesh 3).

x-Momentum conservation:

$$\mathrm{Re}_H\left(u^*\frac{\partial u^*}{\partial x^*}+v^*\frac{\partial u^*}{\partial y^*}+w^*\frac{\partial u^*}{\partial z^*}\right)=-\frac{\partial p^*}{\partial x^*}+\left(\frac{\partial^2 u^*}{\partial x^{*2}}+\frac{\partial^2 u^*}{\partial y^{*2}}+\frac{\partial^2 u^*}{\partial z^{*2}}\right) \tag{6}$$

y-Momentum conservation:

$$\mathrm{Re}_H\left(u^*\frac{\partial v^*}{\partial x^*}+v^*\frac{\partial v^*}{\partial y^*}+w^*\frac{\partial v^*}{\partial z^*}\right)=-\frac{\partial p^*}{\partial y^*}+\left(\frac{\partial^2 v^*}{\partial x^{*2}}+\frac{\partial^2 v^*}{\partial y^{*2}}+\frac{\partial^2 v^*}{\partial z^{*2}}\right) \tag{7}$$

z-Momentum conservation:

$$\mathrm{Re}_H\left(u^*\frac{\partial w^*}{\partial x^*}+v^*\frac{\partial w^*}{\partial y^*}+w^*\frac{\partial w^*}{\partial z^*}\right)=-\frac{\partial p^*}{\partial z^*}+\left(\frac{\partial^2 w^*}{\partial x^{*2}}+\frac{\partial^2 w^*}{\partial y^{*2}}+\frac{\partial^2 w^*}{\partial z^{*2}}\right) \tag{8}$$

Energy conservation for the fluid domain:

$$\mathrm{Pe}_H\left(u^*\frac{\partial \Theta_f^*}{\partial x^*}+v^*\frac{\partial \Theta_f^*}{\partial y^*}+w^*\frac{\partial \Theta_f^*}{\partial z^*}\right)=\frac{\partial^2 \Theta_f^*}{\partial x^{*2}}+\frac{\partial^2 \Theta_f^*}{\partial y^{*2}}+\frac{\partial^2 \Theta_f^*}{\partial z^{*2}} \tag{9}$$

It should be noted that we had established that convective cooling is dominant as compared to natural convective cooling. The governing equations were nondimensionalized using the following

$$u^*=\frac{u}{u_m},\quad v^*=\frac{v}{u_m},\quad w^*=\frac{w}{u_m},\quad p^*=\frac{pH}{\mu_f u_m},$$
$$\mathrm{Re}_H=\frac{\rho_f u_m H}{\mu_f},\quad \mathrm{Pe}_H=\frac{\rho_f c_{pf} u_m H}{k_f} \tag{10}$$

The cooling fluid enters the 3D IC package at ambient temperature with a specified Reynolds number where the characteristic length is the height of the 3D package excluding the heat sink. At the channel outlet, the cooling fluid is assumed to exit the package at atmospheric pressure with negligible streamwise temperature gradient. Moreover, an extended numerical boundary condition is used for the outlet in order to obtain a solution that is not affected by the outflow boundary conditions [20,21]. The outlet boundary conditions are as follows

$$p_o=1\ \text{atm},\quad \frac{\partial \Theta_f^*}{\partial x^*}=0 \tag{11}$$

Based on the pertinent thermal analysis of 3D ICs, the range and nominal values for different components of the 3D IC such as material selection, dimensional attributes, number of layers, etc. are given in Table 1. Silicon is the preferred material used for fabricating electronic chips due to stability, abundancy and ease of fabrication, while copper is preferred for manufacturing heat sink and heat spreader components due to its superior thermal conductivity. The TIM layers, which provide electrical insulation and mechanical support for the bonding of active device layers, are typically made out of composites with high volume fractions of thermally conductive fillers such as Aluminum Oxide (Al_2O_3). The thermal conductivity of TIM layers, made from thermal grease, ranges between 0.2 and 15 [$W\,(m{\cdot}K)^{-1}$] depending on the material and volume fraction of the filler. In this study, we use a nominal value of 5 [$W\,(m{\cdot}K)^{-1}$] for the thermal conductivity of the TIM layer based on the range of values utilized in the literature. As mentioned earlier, in this work, the variation of pertinent components utilized in the 3D architecture is given in Table 1.

Table 2 shows the range and nominal values for various attributes of TSVs and bumps utilized in the 3D IC structure, based on values obtained from pertinent literature. The references for these attributes are provided within Table 2. Through silicon vias (TSVs) are characterized into three categories of power, signal, and thermal TSVs, where power and signal TSVs act as the electrical and data interconnection between device layers, whereas thermal TSVs are utilized to enhance thermal conduction through different layers of the 3D IC. A way to use the simulation to optimize designs has been shown in the prior literature [42–44].

As TSV interconnections and bumps take up a minor volume fraction of the die and TIM layers, an effective medium approximation can be applied to estimate a more accurate value for the thermal conductivity of these layers. Two different methods were used to estimate the effective thermal conductivity in order to ensure the accuracy of the approximations. The Maxwell Garnett method [22] was applied to determine the effective thermal conductivity of each composite medium using the following equation:

$$\sum_{i=1}^{N}\delta_{V_i}\frac{k_i-k_\varepsilon}{k_i+(N-1)k_\varepsilon}=0 \tag{12}$$

where δ_{V_i} and k_i are the volume fraction and thermal conductivity of each constituent, and N, and k_ε denote the system dimension and effective thermal conductivity of the composite medium, respectively. The volume fraction of TSVs and bumps are calculated based on the quantity and dimensions listed in Table 2 and then used in Eq. (12) to approximate the effective thermal conductivity.

Another method developed by Tien and Vafai [23], was also employed, which establishes the following equation for estimating the effective thermal conductivity:

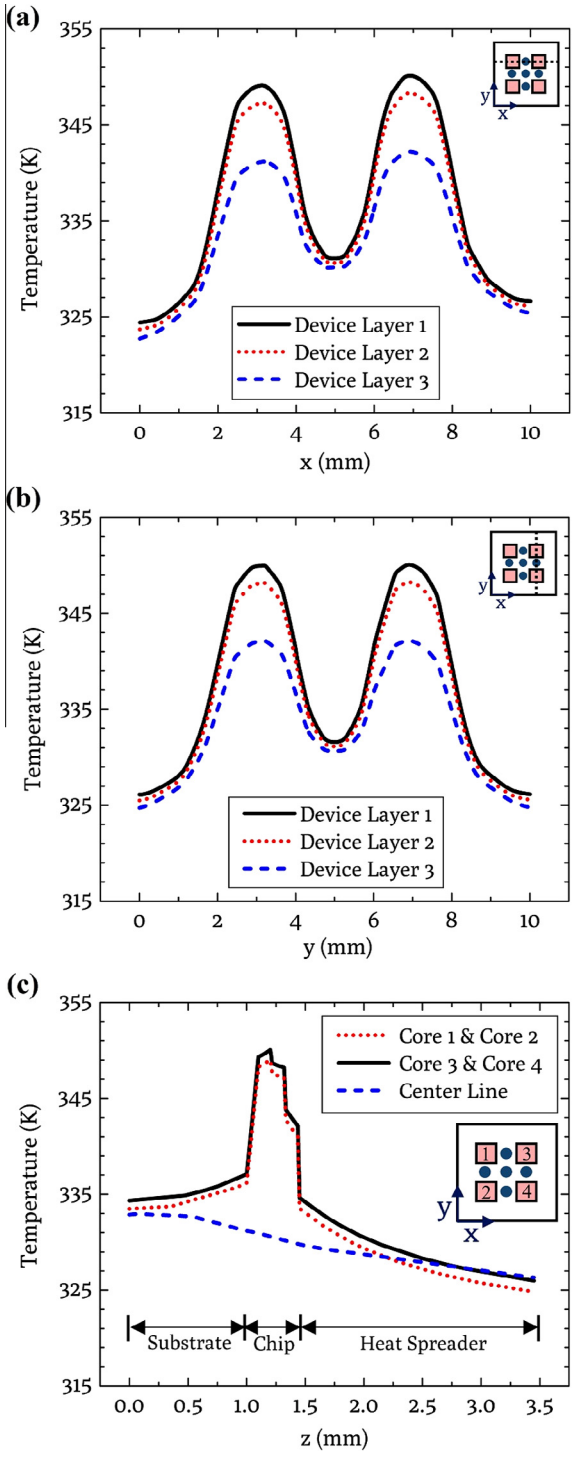

Fig. 5. Temperature distribution for the nominal benchmark 3D IC (a) along x direction for each device layer (b) along y direction for each device layer (c) along z direction at the vertical center line of each core and the center line of chip.

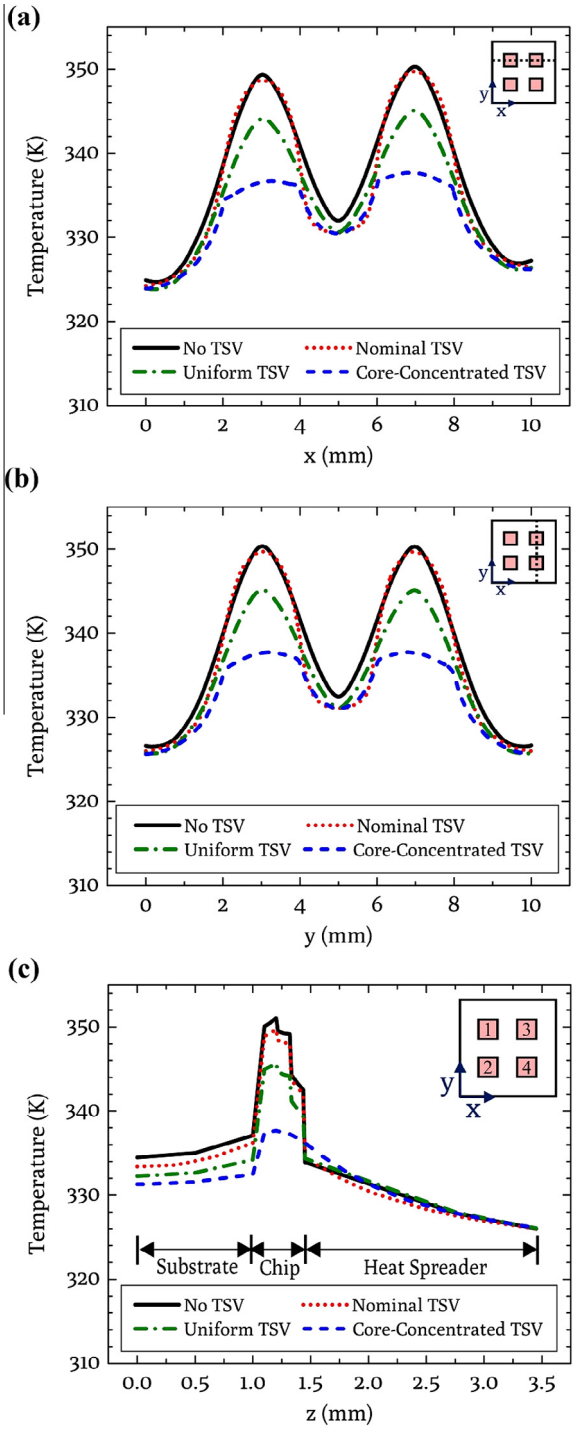

Fig. 6. Effect of different TSV arrangement on the temperature distribution of the 3D IC structure (a) along x direction in device layer 1 (b) along y direction in device layer 1 (c) along z direction at vertical center line of core processor 3.

$$A \leqslant \frac{k_e}{\sqrt{k_1 k_2}} \leqslant B \tag{13}$$

where

$$A = \sqrt{\beta}\left\{\beta - \delta_V(\beta-1) - \frac{(1-\beta)^2\delta_V(1-\delta_V)}{2(1-\beta)\delta_V + 2\beta + 4(\beta-1)(2\delta_V-1)G}\right\}^{-1} \tag{14}$$

$$B = \frac{1+\delta_V(\beta-1)}{\sqrt{\beta}}\left\{1 - \frac{\left[\delta_V(1-\delta_V)(\beta-1)^2\right]}{2[1+\delta_V(\beta-1)][1+(\beta-1)\delta_V + 2(\beta-1)(1-2\delta_V)G]}\right\} \tag{15}$$

and β represents the ratio of the thermal conductivity of two constituents ($\beta = k_1/k_2$), and δ_V denotes the volume fraction of the component with thermal conductivity of k_1. The mean value of the inequality represented by $\frac{k_e}{\sqrt{k_1 k_2}} = \frac{A+B}{2}$ is used as the effective

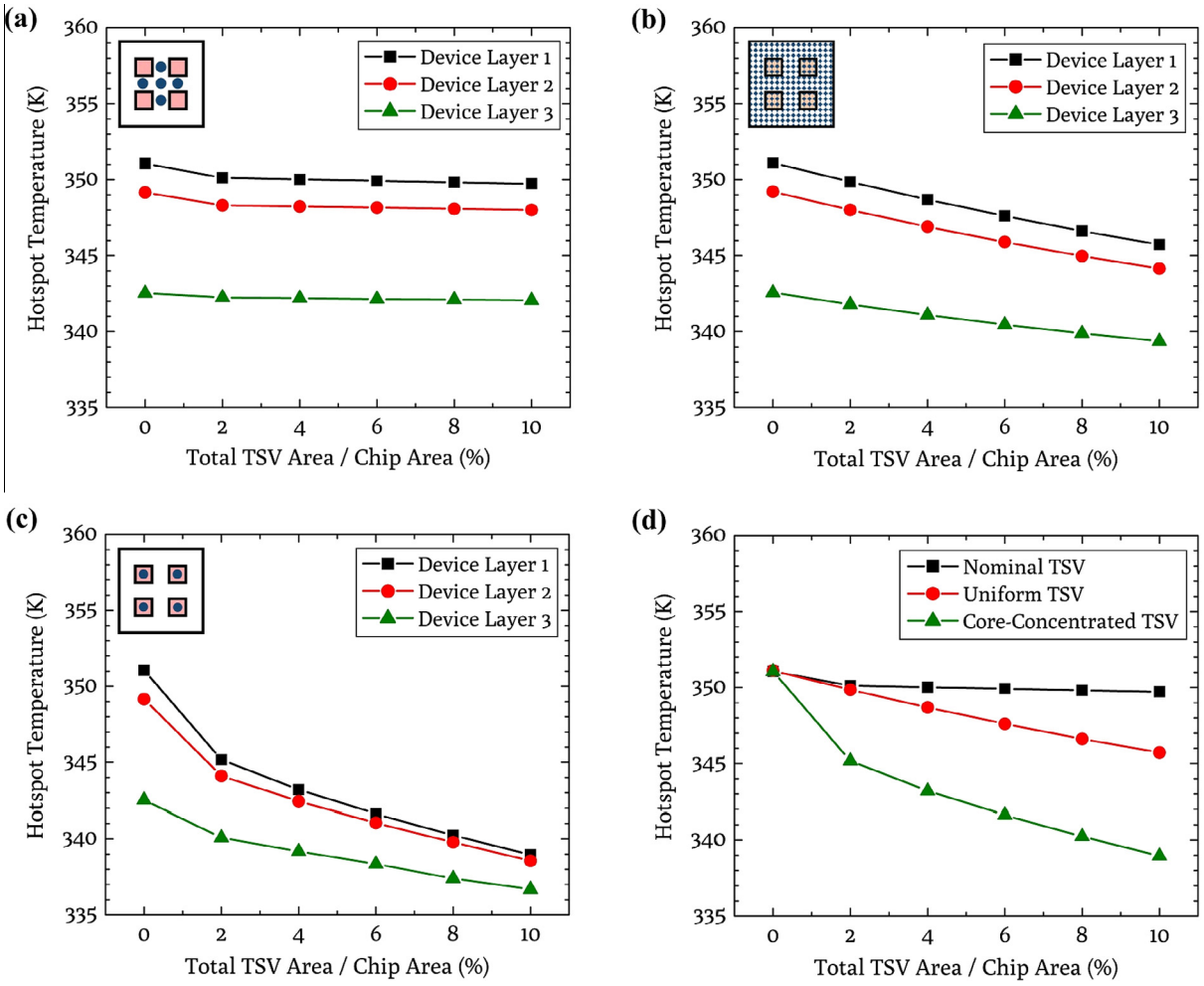

Fig. 7. Effect of the thermal TSV arrangement on the hotspot temperature for (a) nominal TSV (b) uniform TSV (c) core-concentrated TSV (d) various TSV arrangements for device layer 1.

thermal conductivity of medium. Table 3 displays a comparison of the effective thermal conductivity obtained using the two methods. As it can be seen, the results are quite close. In this study, the effective thermal conductivity is estimated using the Tien and Vafai's approach.

3. Modeling validation

COMSOL Multiphysics software is used to model our setups and for numerical simulation of our results. To validate our model, two limiting configurations are compared with our simulations. The first one is a two-dimensional conduction within a slab. Fig. 2a displays the small schematic of the conduction problem where $L = 2$ mm and $d = 3$ mm within the comparison figure. The top boundary has a temperature distribution of $T = f(x)$, while other boundaries are at constant temperature $T = 0$. The temperature distribution across the solid domain is represented by the following analytical solution:

$$T(x,y) = \sum_{n=1}^{\infty} a_n \sin\left(\frac{n\pi x}{L}\right) \sinh\left(\frac{n\pi y}{L}\right) \tag{16}$$

where

$$a_n = \frac{\frac{2}{L}\int_0^L f(x)\sin\left(\frac{n\pi x}{L}\right)dx}{\sinh\left(\frac{n\pi d}{L}\right)} \tag{17}$$

The numerical and analytical results are obtained for three different functions of $f(x)$, which are as follows:

$$f_1(x) = 2x, \quad f_2(x) = 5x^2, \quad f_3(x) = \sin\left(\frac{3\pi x}{L}\right) \tag{18}$$

For each $f(x)$ specification, the temperature distributions along x direction are compared at two different y positions. The comparisons, displayed in Fig. 2, shows excellent agreement between the numerical and analytical results.

The second configuration is based on the study of convective cooling of heated obstacles in a channel by Young and Vafai [16]. The schematic of the model, where the height and width of the obstacle are $h = 0.25$ mm and $w = 0.25$ mm, respectively and the channel dimensions are $H = 1$, $L_e = 2$, $L_o = 8$ is shown within Fig. 3a. The solid-to-fluid thermal conductivity ratio is $k_s/k_f = 10$ and the bottom surface of the obstacle is heated with constant heat flux of $q'' = 1$. The fluid enters the channel with a Reynolds number of $\mathrm{Re}_H = 1000$ where the characteristic length is $2H$. The dimensionless temperature profile, obtained from our simulation, is compared with the results from Young and Vafai [16] in Fig. 3, where very good agreement can be seen between the results. In addition, the local Nusselt number along the surface of the obstacle is also compared in Fig. 3, where the local Nusselt number is defined as:

$$Nu_x = \frac{h_c H}{k_f} = \frac{-1}{\theta_w}\frac{\partial \theta_f}{\partial n} \tag{19}$$

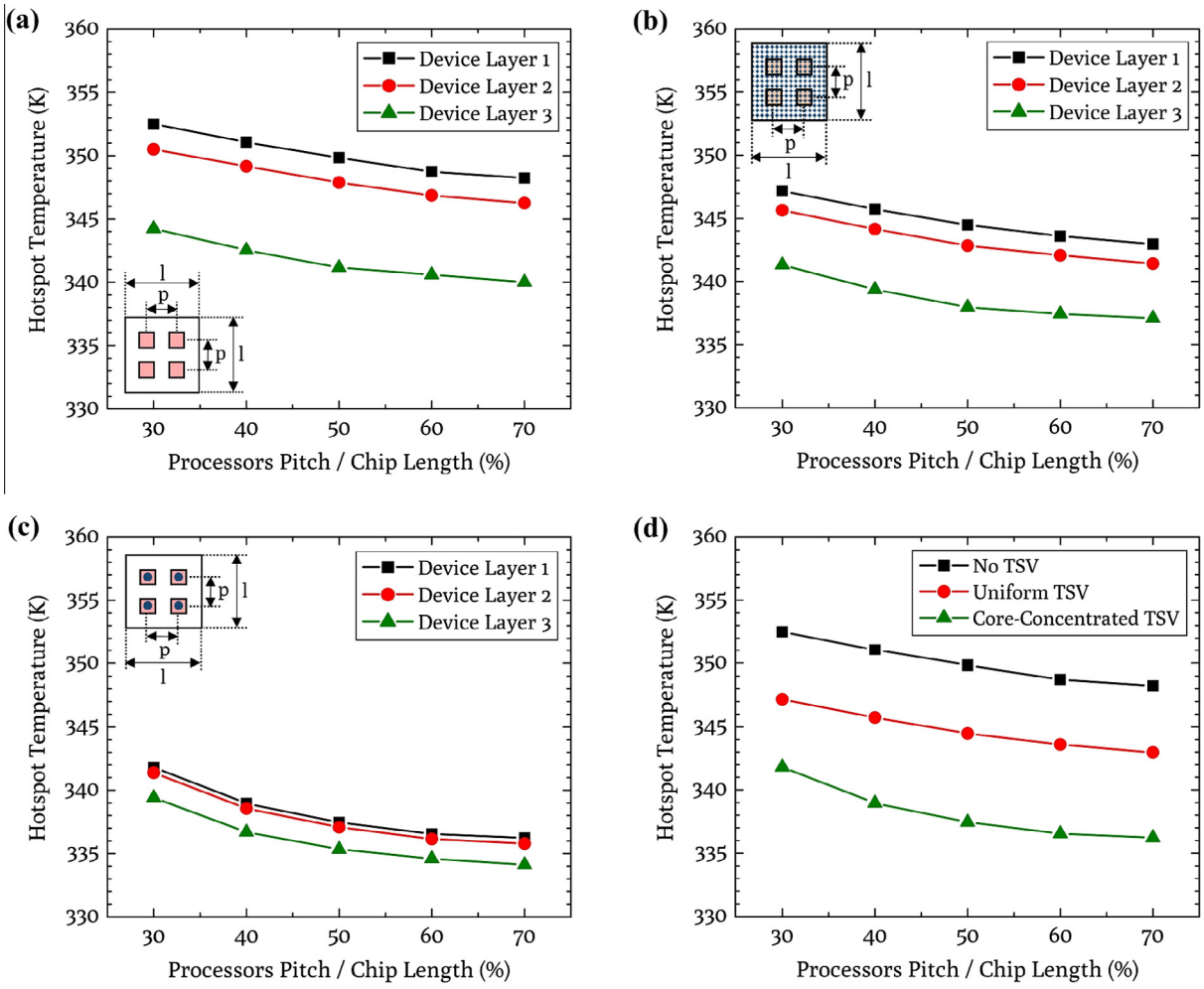

Fig. 8. Effect of processors pitch on the hotspot temperature for (a) No TSV (b) uniform TSV (10% of total chip area) (c) core-concentrated TSV (10% of total chip area) (d) various TSV arrangements (10% of total chip area) for device layer 1.

The local Nusselt number results, obtained by our simulations, are in excellent agreement with those obtained by Young and Vafai [16].

4. Grid independence study

To establish grid independence in our simulations, three different mesh distributions were investigated. The finer mesh (mesh 2) had nearly 75% increase in the number of elements over the coarsest mesh (mesh 1), and the finest mesh had about 50% increase in the number of elements over the finer mesh (mesh 2). Fig. 4 shows the grid independence analysis for these three grid distributions for ten different cases. These ten cases were chosen to demonstrate a wide range of variations in the pertinent physical parameters utilized in our investigations as displayed in Fig. 4. As it can be seen, the deviations in the maximum temperature obtained by applying mesh 2 and 3 is less than 0.1%. As such mesh 3 was adopted for our simulations.

5. Results and discussion

The temperature distribution in the x and y directions as well as at different layers for the nominal benchmark case, based on Tables 1 and 2, is shown in Fig. 5. The location for the temperature distribution for Fig. 5a and b is clearly specified in the inset, within each of these figures. It should be noted that the circles on the insets refer to the position of thermal TSVs, which is the nominal arrangement in this figure. As expected, the highest temperature within each processor occurs at its center and also the core processors on device layer 1, which is farthest from heat sink, are exposed to a higher temperature compared to device layers 2 and 3 and consequently at a higher risk of failure, which necessitates a greater attention for thermal management of this layer. The temperature distribution is symmetrical in y direction due to symmetrical boundary conditions on both sides of the 3D IC structure. However, the temperature profile is asymmetrical in x direction as one side is exposed to the incoming cooling fluid, which is relatively colder, since the temperature of cooling fluid increases as it flows in x direction while dissipating heat from the circuit. Fig. 5c displays the temperature distribution of the benchmark 3D IC along the z direction at the centerline of each core and the chip.

As it can be seen, the heat spreader has a lower average temperature compared to the substrate since the convective heat transfer coefficient of the heat sink is forty times greater than that of the substrate ($h_t/h_b = 40$) in the nominal case [24]. Again, as expected, the maximum temperature occurs within device layer 1, where the core processors are farthest from the heat sink. This indicates the dominance of heat sink in cooling the circuit as the heat generated in the core processors is mainly dissipated through the direct and

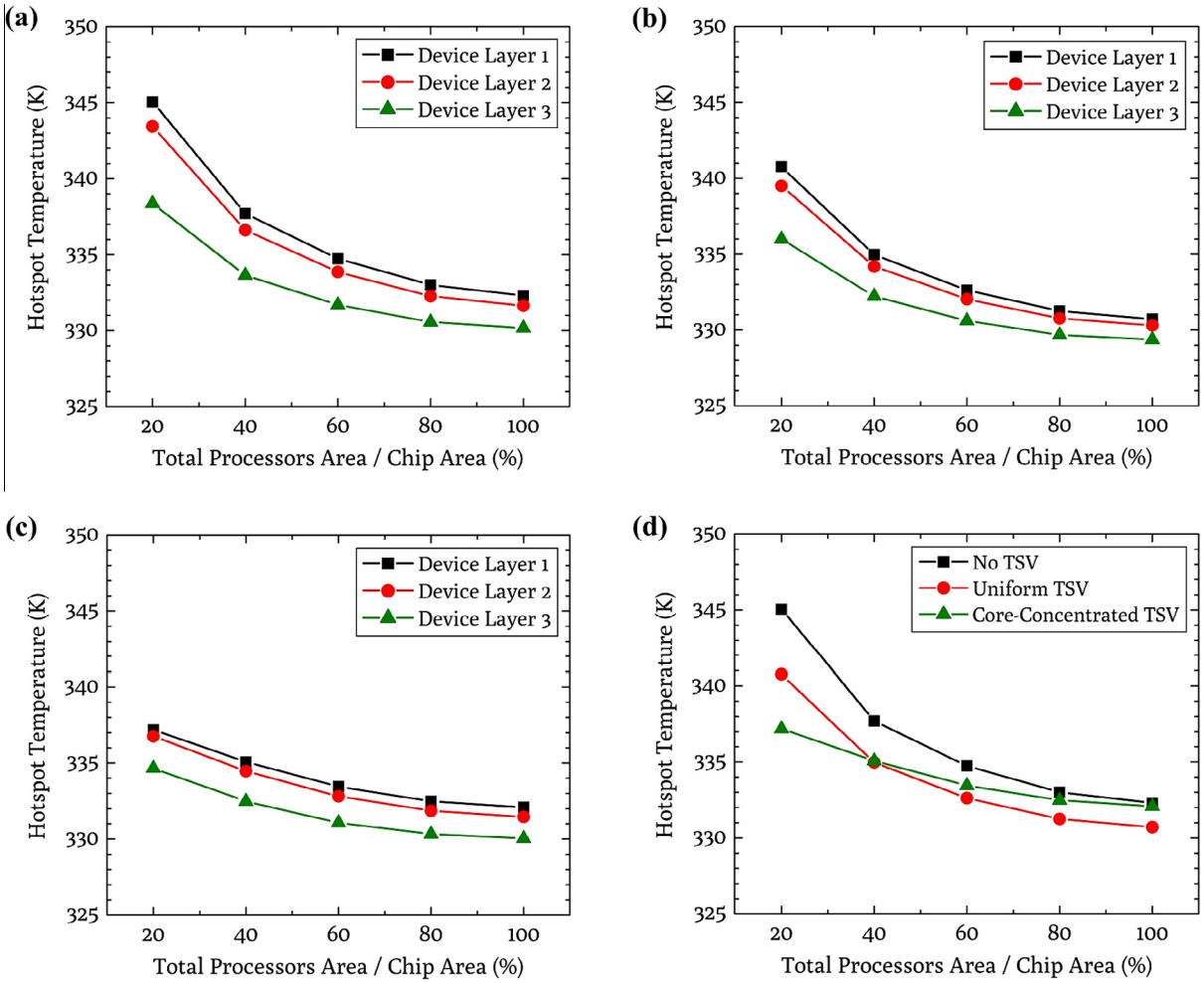

Fig. 9. Effect of the processor area on the hotspot temperature for the same chip area and total heat dissipation for (a) No TSV (b) uniform TSV (10% of total chip area) (c) core-concentrated TSV (10% of total chip area) (d) various TSV arrangements (10% of total chip area).

indirect communication of the layers of the 3D IC with the heat sink and then transferred to the ambient by convection. As Fig. 5c illustrates, temperature gradient along z direction is substantially larger at four regions, which is due to low thermal conductivity of TIM layers that impede conduction of heat between the device layers. In each device layer, the maximum temperature of core 1 and core 2 is lower compared to that of core 3 and core 4, as the former ones are closer to the incoming flow of the cooling fluid.

Fig. 6a and b show the temperature distribution of the 3D IC structure with four different thermal TSV arrangements along x and y directions in device layer 1, which is the most vulnerable layer due to local heat dissipation and farthest away from the heat sink. Again, the location for the temperature distributions for Fig. 6a and b are given in the insets within these figures. As expected, the No TSV case, which assumes no thermal TSV is implemented in the 3D IC structure, has indeed the highest maximum temperature. Interestingly, the nominal TSV scenario that deploys five localized thermal TSVs between the core processor, has minimal thermal impact with less than one degree reduction in peak temperature. It should be noted that all TSV arrangements make up 10% of the total chip area. In the Uniform TSV scenario, where the thermal TSVs are implemented uniformly in each layer, a greater improvement in cooling is achieved with nearly 5 degrees reduction in the maximum temperature compared to the No TSV case.

The core-concentrated TSV case, which deploys concentrated thermal TSVs on top of each core processor, has by far the best thermal performance, as it not only reduces the peak temperature by more than 12 degrees, but also results in a more uniform temperature distribution over each core region that minimizes the thermal stresses. Fig. 6c illustrates how each TSV arrangement affects the temperature distribution along the z direction at the vertical center line of core 3. Although these results indicate that uniformly distributed thermal TSVs can improve the thermal characteristics of the circuit to some extent, this TSV arrangement is outperformed by concentrated thermal TSVs, which enhances conduction in the z direction by concentrating highly-conductive thermal TSVs in the regions where heat is locally generated. In addition, these results show that the core-concentrated thermal TSVs lead to a more uniform temperature distribution along the z direction through optimum placement of thermal TSVs such that heat conduction is maximized and accordingly thermal hotspots are minimized.

Fig. 7 shows the effect of thermal TSVs on the hotspot (maximum) temperature of the 3D IC. It is found that the maximum temperature decreases slightly as the thermal TSVs with the nominal arrangement are implemented (Fig. 7a), however, the maximum

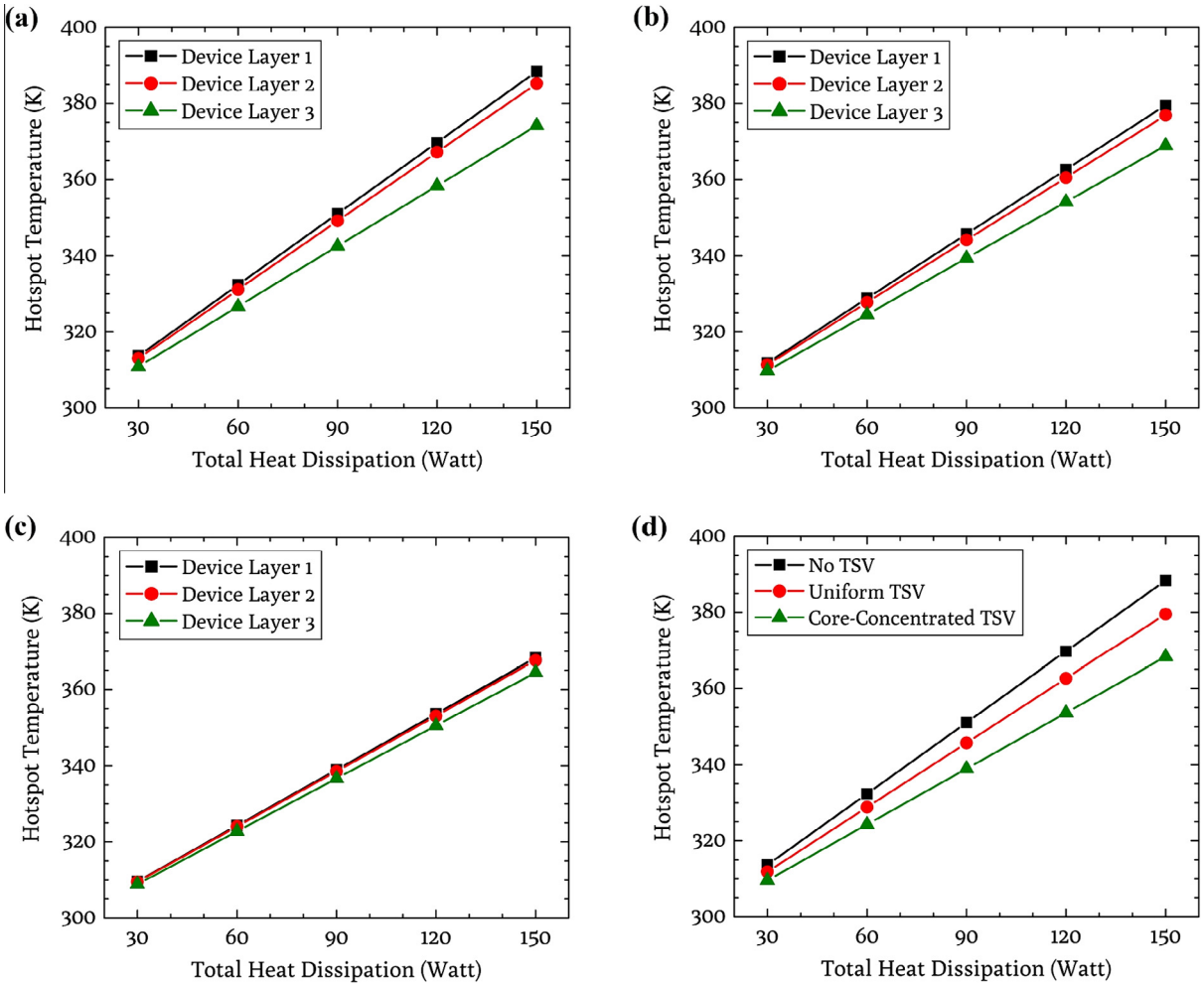

Fig. 10. Effect of the total heat dissipation on the hotspot temperature for (a) No TSV (b) uniform TSV (10% of total chip area) (c) core-concentrated TSV (10% of total chip area) (d) various TSV arrangements (10% of total chip area).

temperature remains nearly constant as the TSV area increases showing the insignificant effect of increasing the number of TSVs for this case. On the other hand, when the total area of uniformly distributed thermal TSVs increases, the hotspot temperature decreases linearly leading to a nearly half degree drop in the maximum temperature for each percent increase in the TSV area. The core-concentrated TSV arrangement has superior thermal performance with a decrease of the maximum temperature by more than 5 °C when the total TSV area is only 2% of the chip area. In addition, the peak temperature in each device layer decreases linearly as the total TSV area increases, resulting in greater temperature uniformity between the device layers. Fig. 7d compares the effect of different TSV arrangements on the maximum temperature of the device layer 1 displaying the superior performance of the core-concentrated TSVs for dissipating local heat generation in core processors.

Fig. 8 displays the effect of core processors pitch on the maximum temperature of each device layer for different TSV arrangements. It is found that for all TSV arrangements, the hotspot temperature drops as the pitch increases. This is due to the fact that the greater pitch not only leads to less accumulation of heat generated by processors in a localized region, but also results in enhanced cooling through convection heat transfer to the cooling fluid. Fig. 8d compares the dependency of hotspot temperature on the core processors pitch for various thermal TSV arrangements for device layer 1. It is found that the pitch variations has a similar effect on different TSV arrangements.

The effect of the size of the core processors on the hotspot temperature for various TSV arrangements, when the chip area and total heat dissipation remain constant, is shown in Fig. 9. As expected, for all TSV arrangements, the hotspot temperature drops as the processor area increases since the same amount of heat is dissipated over a larger volume leading to less localization of heat and accordingly lower maximum temperature. As Fig. 9d illustrates, the hotspot temperature for the No TSV case drops at a greater rate compared to the core-concentrated TSV, resulting in equal hotspot temperature for both TSV arrangements when core processors take the entire chip area or, in other words, when the heat dissipation is uniform throughout the chip. In addition, this figure indicates that uniform TSV arrangement outperforms core-concentrated TSVs when the total processor area is greater than 40% of the chip area. This is due to the fact that a core-concentrated TSV has a superior performance when the heat generation of core processors is localized, while, a uniform TSV arrangement results in better thermal characteristics when the heat generation is uniformly distributed throughout the chip area.

The effect of heat dissipation by the 3D IC structure on the hotspot temperature in lieu of different TSV arrangements is displayed in Fig. 10. As expected, regardless of the TSV arrangement, the maximum temperature of the 3D structure increases as the total

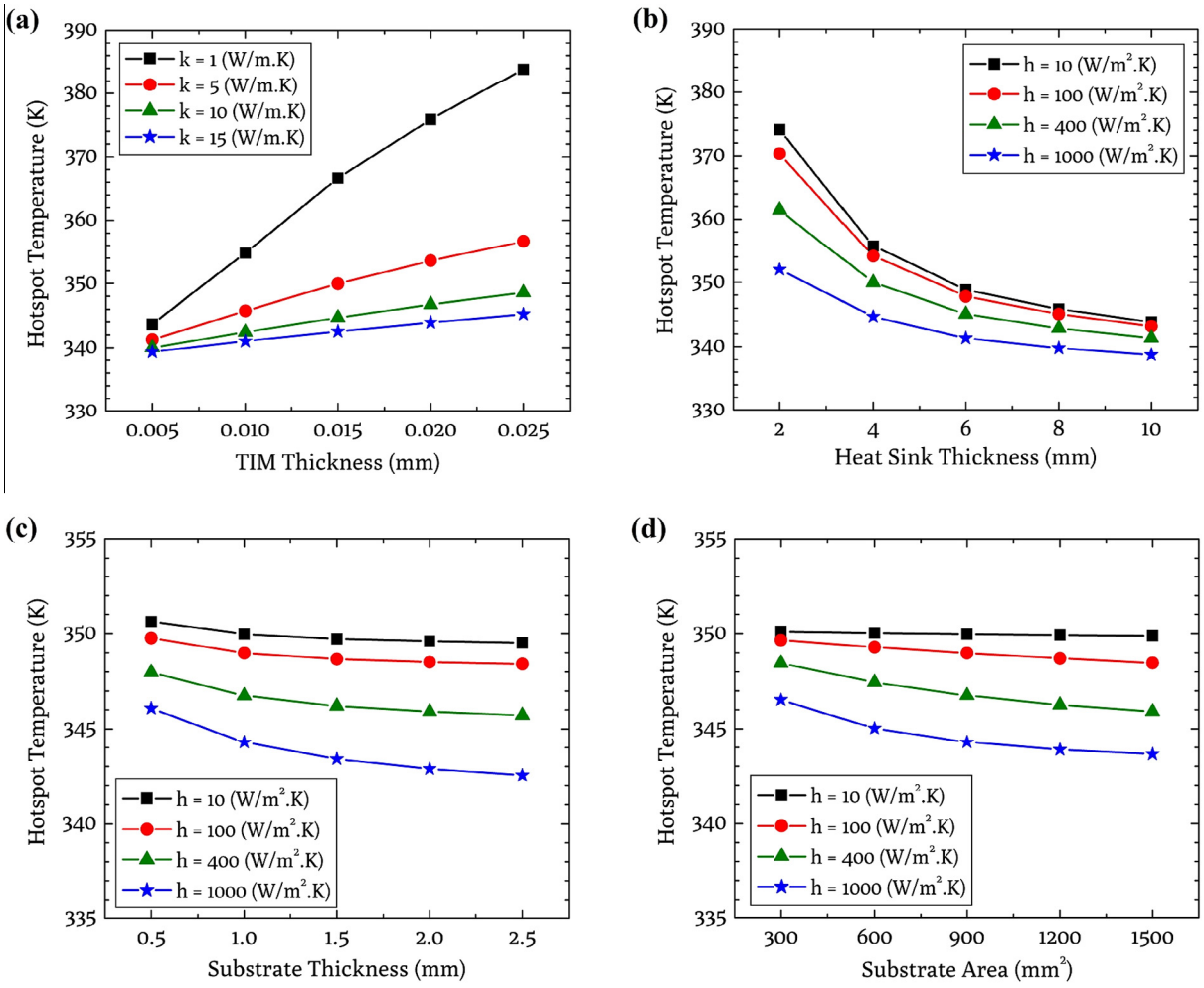

Fig. 11. Alteration of the hotspot temperature through (a) TIM thickness and thermal conductivity (b) heat sink thickness (c) substrate thickness (d) substrate area.

heat dissipation increases. As can be seen in Fig. 10, the temperature variation between the device layers diverge as the total heat dissipation increases, however, the hotspot temperature differences within the three device layers for the core-concentrated scenario is relatively negligible. The thermal performance of various TSV arrangements at different heat dissipation rates in terms of the hotspot temperature is shown in Fig. 10d. Our results show the importance of deploying core-concentrated TSVs in 3D ICs at higher heat dissipation rates.

Alterations of the hotspot temperature through TIM thickness and thermal conductivity, heat sink thickness, and substrate thickness and area variation is shown in Fig. 11. As can be seen, the hotspot temperature rises as the TIM thickness increases due to relatively low thermal conductivity of TIM material and as expected, the increase in the hotspot temperature is more severe when the thermal conductivity of the TIM material is smaller. This result reiterates the importance of utilizing a TIM material with larger thermal conductivity and a smaller thickness. The effect of heat sink thickness and convective heat transfer coefficient on the hotspot temperature is shown in Fig. 11b. It can be seen that increasing the thickness of the heat sink lowers the hotspot temperature nonlinearly resulting in a minima such that thermal characteristics are not enhanced beyond a given thickness of the heat sink. The maximum hotspot temperature drop occurs if a heat sink with 10 mm thickness is deployed. Furthermore, the effect of convective heat transfer coefficient becomes less significant when the optimum thickness of the heat sink is utilized. Fig. 11c and d display the effect of substrate thickness, surface area, and convective heat transfer coefficient on the hotspot temperature of the 3D IC structure. It should be noted that increasing the substrate surface area and thickness has a relatively negligible effect on the hotspot temperature within the customary range of convective heat transfer coefficients experienced within the 3D structure. Increasing the substrate dimensions can significantly improve the thermal characteristics and reduce the hotspot temperature only when the convective heat transfer coefficient is extremely large.

Fig. 12a presents a detailed case study for evaluating the dependency of hotspot temperature on distribution of power among the device layers. In the nominal case, all device layers have equal functionality and heat dissipation (30 W each), while in the other scenarios, one of the device layers has a greater functionality and accordingly higher heat dissipation. The power is equally distributed amongst all core processors within each device layer. As it can be seen in Fig. 12b, the hotspot temperature is minimized when the majority of processing is performed by the core processors on device layer 3 (cases D3 and D6), which is the closest one to the heat sink, regardless of the utilized TSV arrangement. In contrast, the thermal characteristics are worsened compared to the nominal case if most of the processing chores are accomplished by the core processor on device layer 1 (cases D1 and D4), which is the farthest one from the heat sink. On the other hand, the task load within the device layer 2 (cases D2 and D5) has a minimal impact on the thermal performance of the 3D structure.

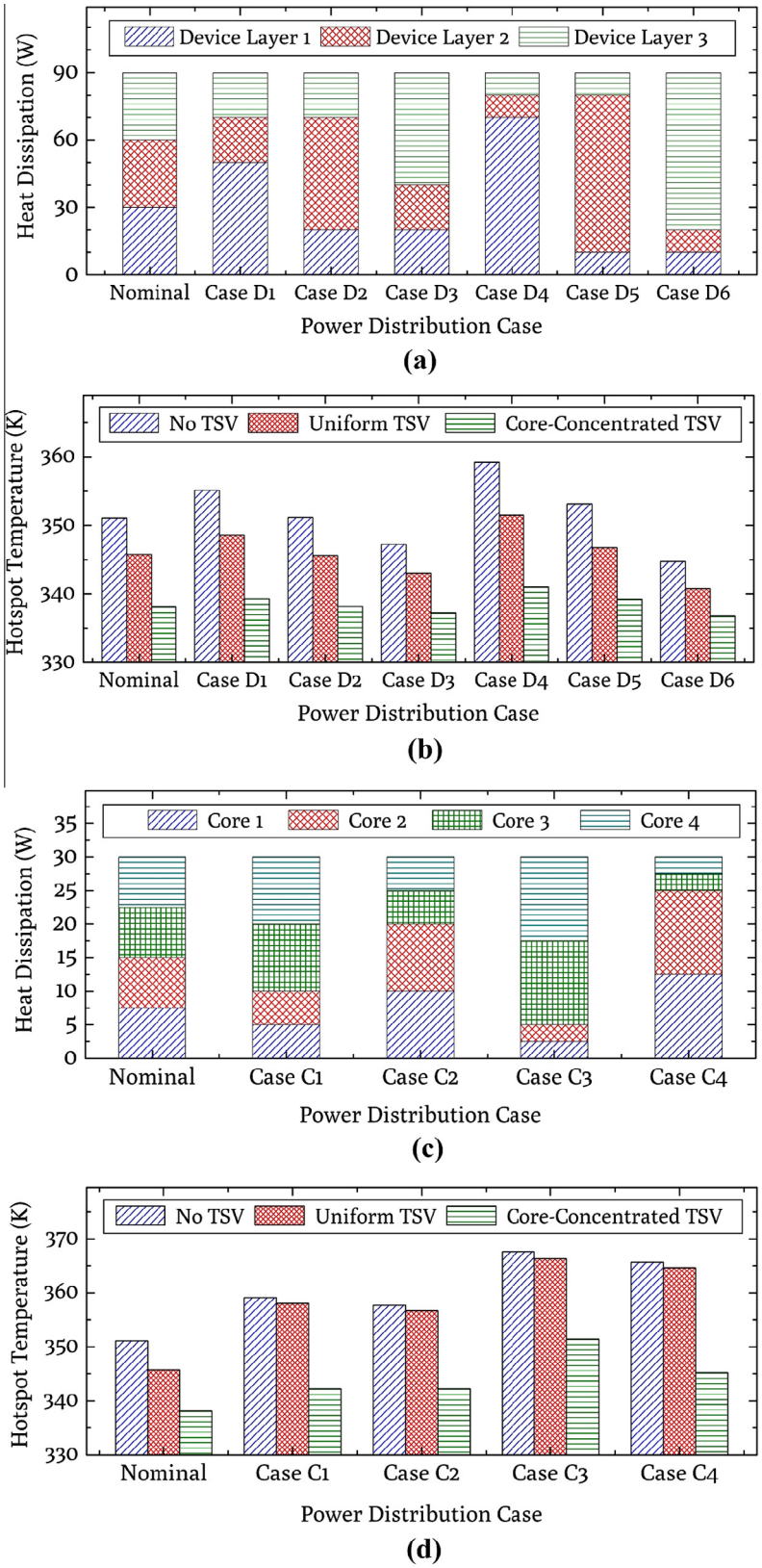

Fig. 12. (a) Case study for the power distribution within the device layers (b) effect of the power distribution within the device layers on the hotspot temperatures (c) case study for power distribution within the cores of each device layer (d) effect of the power distribution within the cores of each device layer on the hotspot temperature.

Fig. 12c displays a case study for investigating the effect of power distribution among the core processors for each device layer on the hotspot temperature. In the nominal case, power is uniformly distributed among the core processors for each device layer i.e. each core dissipates 7.5 W, while in the other scenarios, two cores have greater functionality and accordingly larger heat

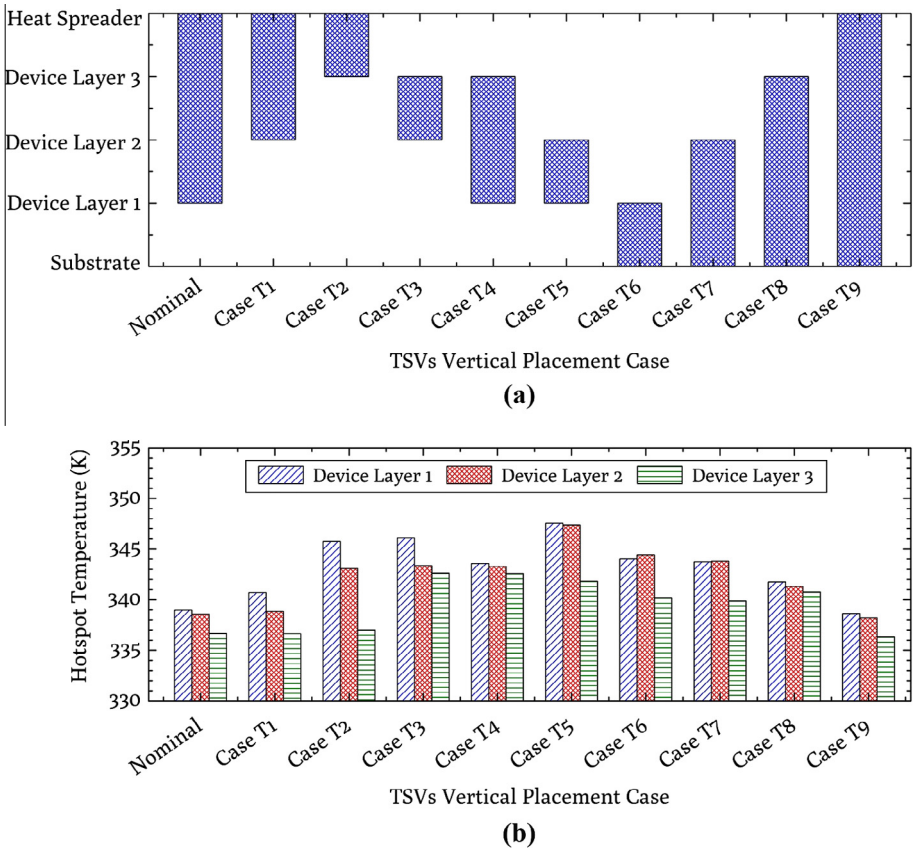

Fig. 13. (a) Case study for the vertical placement of the core-concentrated TSVs with a 10% of chip area (b) effect of the vertical placement of the core-concentrated TSVs on the hotspot temperature in each device layer.

dissipation compared to others. In this part, when variable distribution amongst different core processors is applied, it is imposed on all the device layers. Fig. 12d shows that non-uniform distribution of power among the cores of each device layer deteriorates the thermal characteristics and increases the hotspot temperature, regardless of the utilized TSV arrangement. Therefore, the optimum setup for reducing the hotspot temperature is achieved if power is evenly distributed among the core processors of each device layer in the 3D IC.

Fig. 13 presents a case study for evaluating the effect of vertical placement of the core-concentrated thermal TSVs, which were found to provide the best thermal performance based on our earlier presented results, on the hotspot temperatures. It is found that implementing core-concentrated thermal TSVs through all layers of the 3D IC structure will result in the optimum thermal performance and the minimum hotspot temperature (case T9).

The effect of adding additional layers on the hotspot, while imposing the same total power generation within the 3D IC is displayed in Fig. 14. It can be seen that, when core-concentrated thermal TSVs are implemented, an increase in the number of layers beyond 3 does not have much of an impact on the hotspot temperature within the 3D IC. This is an unexpected interesting finding. In fact, increasing the number of layers could have an adverse effect on the hotspot temperature when No TSV or uniform TSV is employed.

6. Summary and conclusions

In this work, a comprehensive and systematic study of the critical thermal issues in the 3D ICs is presented. A nominal 3D IC structure based on the data from pertinent literature is developed and the effects of various prominent parameters such as different TSV arrangements, processor pitch, processor area variations, heat dissipation variation and distribution, TIM thickness and thermal conductivity variation, heat sink and substrate thickness and area variations, power distribution within different device layers, variations within different core processors, and variations in TSV placement within the 3D layers for the optimized arrangement as well as the effect of additional layers are analyzed in detail. A set of guidelines for achieving optimum thermal characteristics are established and the pertinent attributes of the optimum 3D IC design are presented. The following key features were established through our comprehensive analysis:

1. The device layer closest to the substrate is the most critical one in terms of the hotspot temperature production under various conditions considered in this study.
2. The utilization of the core-concentrated TSV provides the optimum arrangement for reducing the hotspots, resulting also the best arrangement when increasing the total TSV area.
3. An increase in the pitch relative to the chip length will in general result in a reduction of the hotspot temperature regardless of the device layer and the TSV arrangement.
4. As expected, for the same power density, an increase in the processor area relative to the chip will result in a reduction in the hotspot temperature regardless of the TSV configuration. When the processor area is greater than 40%, the uniform TSV arrangement outperforms the core-concentrated arrangement, while below 40%, it is the other way around.

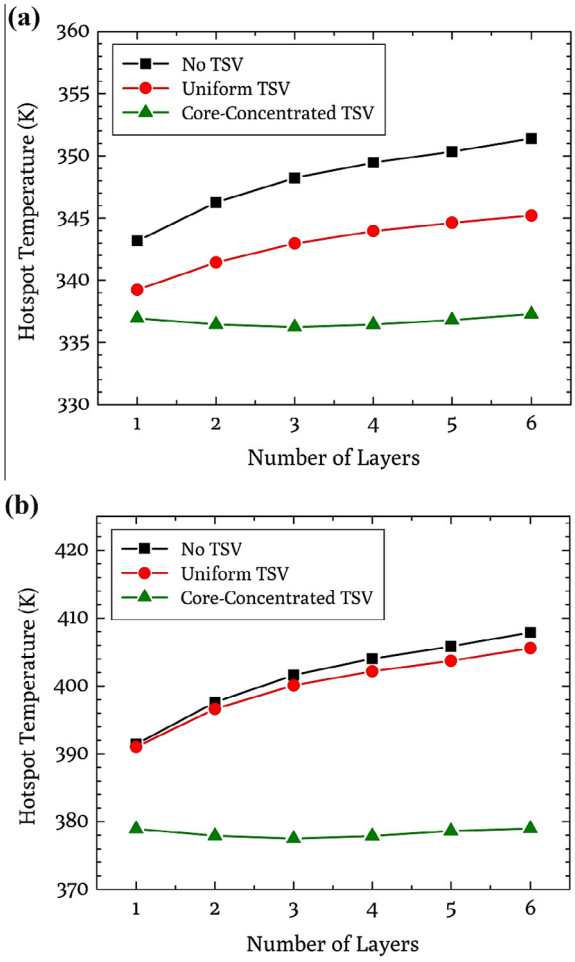

Fig. 14. Effect of the number of layers on the hotspot temperature for (a) 90 W total heat dissipation (b) 180 W total heat dissipation.

5. As expected, an increase in the power dissipation of the device layers will translate into an increase in the chip temperature while the temperature difference between the different layers for the core-concentrated TSV arrangement becomes negligible.
6. An increase in the TIM thickness results in an increase in the hotspot temperature while an increase in the heat sink thickness or the substrate thickness or their areas results in a reduction of the hotspot temperature.
7. It is established that the best performance in terms of the reduction in the hotspot temperature occurs when more of the processing is delegated to the device layer closest the heat spreader.
8. It is established that non-uniform power distribution amongst the processors within a device layer, deteriorates the thermal characteristics in terms of the hotspot temperature.
9. It is established that the best emplacement of the optimized TSV arrangement, which was found to be the core-concentrated, is when the TSVs go through all layers of the 3D IC structure.
10. It is established that additional layers beyond 3 for the same total power dissipation have an insignificant effect on the hotspot temperature, if core-concentrated TSV arrangement is utilized.

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